Multivibrators

Multi means many ; vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are 3 types of multivibrators

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

A bistable multivibrator requires a triggering signal to change from one stable state to another. As the name indicates, a bistable multivibrator has two stable states. A monostable multivibrator has only one stable state. (the other state is being quasi stable). And the astable multivibrator has no stable states (both states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. only when a proper external triggering signal applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

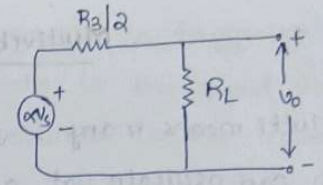
Bistable multivibrator requires a triggering signal to change from one stable state to another. It requires another triggering signal for the reverse transition.

The output voltage is given by

$$v_o = \alpha v_c \times \frac{R_L}{R_L + (R_3 | 2)}$$

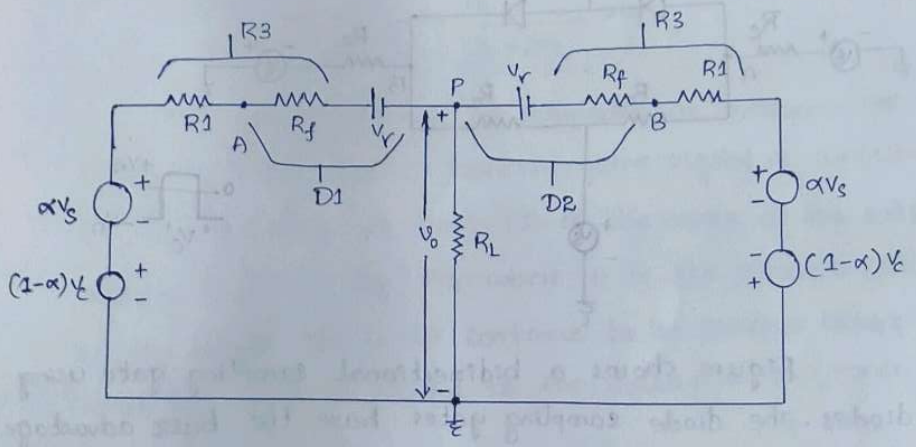
$$A = \frac{v_o}{v_s} = \alpha \cdot \frac{R_L}{R_L + (R_3 | 2)}$$

$$A = \frac{R_C}{R_C + R_2} \cdot \frac{R_L}{R_L + (R_3 | 2)}$$



Thevenins equivalent circuit

Gain : The gain of the sampling gate defined as the ratio v_o/v_s during the transmission interval can be easily calculated from the equivalent circuit as shown below.



$$R1 = R_2 \| R_c = \frac{R_2 R_c}{R_2 + R_c} \quad ; \quad R_3 = R_1 + R_f \quad ; \alpha = \frac{R_c}{R_2 + R_c}$$

each diode has been replaced by its piecewise linear model i.e a battery of V_r equal to the offset voltage in series with a resistance R_f equal to the diode forward resistance. from the equivalent circuit we can observe that the offset voltages V_r and V_r and the control voltage components $(1-\alpha)V_c$ and $(1-\alpha)V_c$ try to send equal currents in opposite directions in R_L and hence the net current due to them is zero. The open circuit voltage at 'p' with respect to ground is αV_s (because all other sources are to be neglected) and the theumin's equivalent resistance at 'p' with respect to ground is $R_3/2$.

Bidirectional sampling gate :

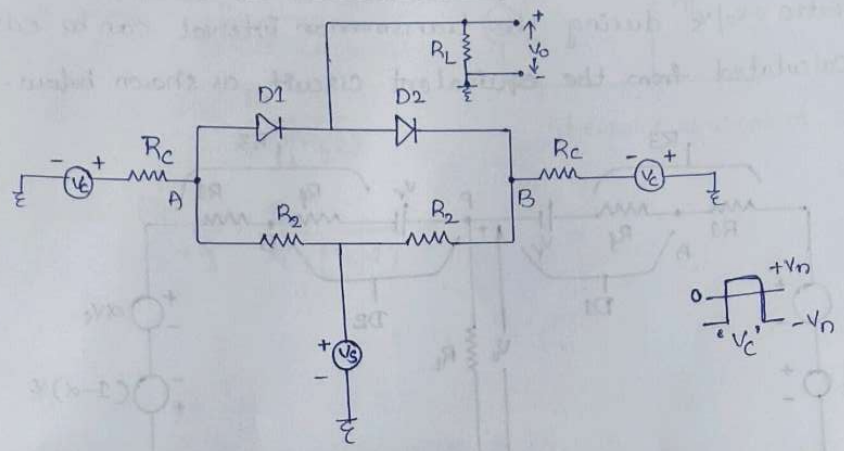


Figure shows a bidirectional sampling gate using diodes. The diode sampling gates have the basic advantage of linearity of operation. Also they canbe adjusted easily to obtain zero pedestal. Two symmetrical gating voltages $+V_c$ and $-V_c$ are connected to the circuit. The control signals are at the levels $+V_n$ and $-V_n$ respectively. The signal at 'A' is $-V_n$ and the signal at 'B' is $+V_n$. So both the diodes are reverse biased and hence no signal transmission takes place. When the control signals are at the levels of $+V_c$ and $-V_c$ i.e when the signal at 'A' is $+V_c$ and the signal at 'B' is $-V_c$, both the diodes D1 and D2 are ON and then a sample of V_s appears at the output. If the diodes are identical in characteristics because of the symmetry in the circuit, no pedestal can appear at the output in response to the control voltages.

diode sampling gate is given by

$$A = \frac{R_c}{R_c + R_2} \times \frac{R_L}{R_L + (R_3/2)}$$

and $$V_{min} = \frac{R_c}{R_2} \times \frac{R_3}{R_3 + 2R_L} \times V_s$$

The voltage $(V_c)_{min}$ is computed as follows. Assuming that $R_f << R_L$, for a positive going signal of amplitude V_s, the voltage at point P1 is the same as the output voltage V_o given by AV_s where A is the circuit gain. If the diode D3 is to continue to be reverse biased, V_c must be at least equal to the voltage at P1. Hence,

$$(V_c)_{min} = AV_s$$

The voltage V_n must be selected not only to keep the transmission diodes D1 and D2 reverse biased but also to keep the clamp diodes D3 and D4 conducting in the presence of the signal V_c. The voltage at P2 for a positive signal V_s and hence the minimum value of V_n by applying superposition theorm is

$$(V_n)_{min} = \frac{V_s R_c}{R_c + R_2} - \frac{VR_2}{R_2 + R_c}$$

The four diode sampling gate shown in figure above improves these features. This is obtained by adding two more diodes to the two-diode sampling gate. Two balanced voltages +V and -V are also required.

When the control voltages are V_c and $-V_c$ respective -ly, the diodes D3 and D4 are reverse biased. because of the voltages +V and -V, the diodes D1 and D2 conduct and the signal source is coupled to the load through the resistors R_2 and the conducting diodes D1 & D2. Under these circumstances, the control voltages are disconnected from the gate by the reverse biased diodes D3 and D4, so an imbalance in control signals cannot result in a pedestal at the output.

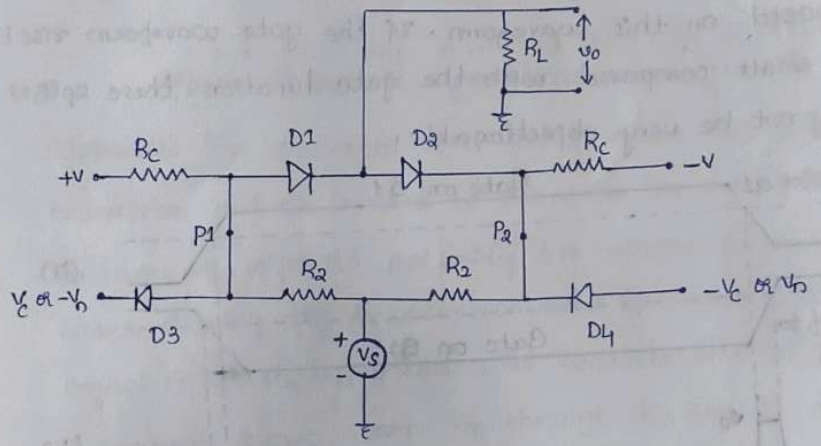
When the control voltages are V_n and $-V_n$, the diodes D3 and D4 conduct and the points P2 and P1 are clamped to these voltages. So the diodes D1 and D2 are reverse biased. Under these circumstances, the output is zero.

Let us now compute the gain A and the required minimum values of V, V_c and V_n. during transmission the diodes D3 and D4 are OFF and the circuit is identical to bidirectional sampling gate except that the voltages $\pm V_c$ are replaced by $+V_c$ and -V respectively. Hence the gain of this circuit is the same as the gain of the two

2. There is a continuous flow of current through R_c and so it has to dissipate a lot of heat.

3. The circuit is complicated. It requires two bias voltages i.e $-V_{BB1}$ and $-V_{BB2}$ and two control signal sources which are complements of each other.

Four diode sampling gate :



Some of the disadvantages of the two-diode sampling gates are

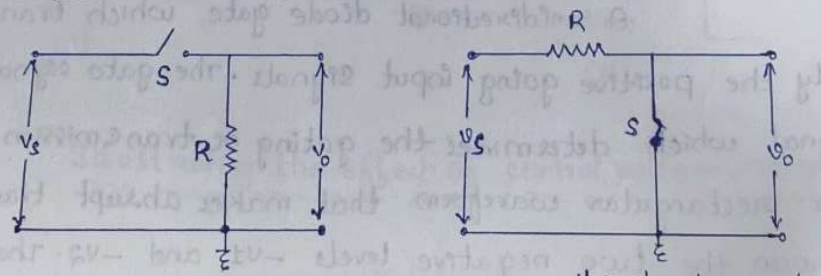
1. Its gain is low.
2. It is sensitive to control voltage imbalance.
3. There is a possibility that $(V_h)_{min}$ may be excessive.
4. There may be appreciable leakage through the diode capacitance.

Sampling gates: Sampling gates also called linear gates, transmission gates or selection circuits, are transmission circuits in which the output is an exact reproduction of the input during a selected time interval and is zero otherwise.

The time interval for transmission is selected by an externally impressed signal which is called the gating signal and is usually rectangular in wave shape. sampling gates may be unidirectional or bidirectional sampling gates. Unidirectional sampling gates are those which transmit signals of only one polarity and bidirectional sampling gates are those which transmit signals of both the polarities

Sampling gates are different from the logic gates. In logic gates there can be any number of inputs and the outputs of the logic gates are either pulses or voltage levels and the output is not a reproduction of the input. The output of a sampling gate is an exact reproduction of the input during the selected time interval.

Basic operating principle of sampling gates:



(a) Series switch (b) Shunt switch

epitaxial silicon transistors may yield saturation voltage as low as 0.2V with collector currents as high as an ampere. On the other hand, the grown junction Ge transistors have saturation voltages which are several tenths of a volt and silicon transistors of this type may have saturation voltages as high as several volts.

Temparature sensitivety of saturation parameters :

At constant base and collector currents, the forward base to emitter voltage $|V_{BE}|$ has a typical temparature sensitivety in the range -1.5 to $-2 mV/^{\circ}C$. This applies both to Ge and Si transistors. A plot for Ge of V_{BE} versus the ambient temparature is shown in fig(a). A similar characte -ristic for silicon has approximately the same slope.

In saturation, the transistor consists of two forward-biased junctions back-to-back series opposing. It is consequently to be anticipated that the temparature induced voltage change in one junction will be cancelled in some measure by the change in the other junction. Such is the case for $V_{BE(sat)}$ as well, as shown in fig(b).

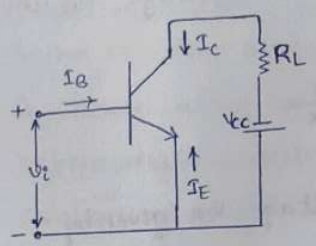
The temparature dependence of h_{fe} is shown in fig(c). At small and moderate currents, h_{fe} increases substantially with temparature. At high currents, h_{fe} may well become rather insensitive to temparature.

necessary to keep V_{cc} correspondingly small inorder to stay within the limitations imposed by the transistor on the maximum current and dissipation. The total voltage swing at the transistor switch is $V_{cc} - V_{CE(sat)}$. The largest possible output swing is desirable inorder to reduce the sensitivity of the switching circuit to noise, supply voltage fluctuations transistor ageing and replacement.

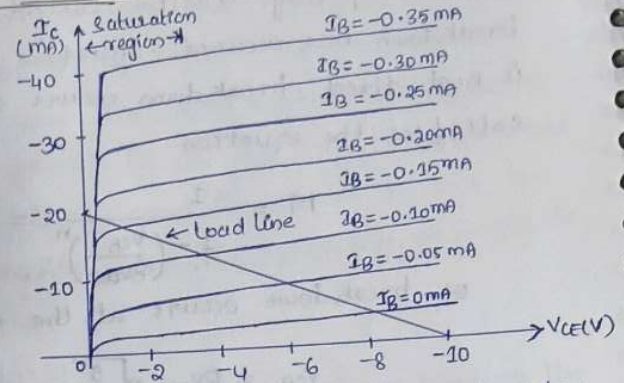
For the transistor switch of fig(a), it is difficult to read $V_{CE(sat)}$ of fig(b). By changing scale, fig(b) can be drawn as shown in fig(c). In these characteristics the 0 to -0.5V region of fig(b) has been expanded and the same load line is drawn. At $I_B = -0.15$ mA, the transistor is in saturation and $|V_{CE}| = 175$ mV. At $I_B = -0.35$ mA, $|V_{CE}|$ has dropped to 100 mV. For a transistor operating in the saturation region, a quantity of interest is the ratio $V_{CE(sat)} / I_C$. This parameter is called the "common emitter saturation resistance", $R_{CE(sat)}$.

The saturation voltage depends not only on the operating point but also on the semiconductor material (Ge or Si) and the type of transistor construction. Alloy-junction transistors and epitaxial transistors gives the lowest values for $V_{CE(sat)}$, whereas the grown junction transistors yield the highest. Germanium transistors have lower values for $V_{CE(sat)}$ than those for silicon. An alloy junction Ge transistor may allow, with adequate base currents, values for $V_{CE(sat)}$ as low as tens of millivolts at collector currents which are some tens of milliamperes. Similarly

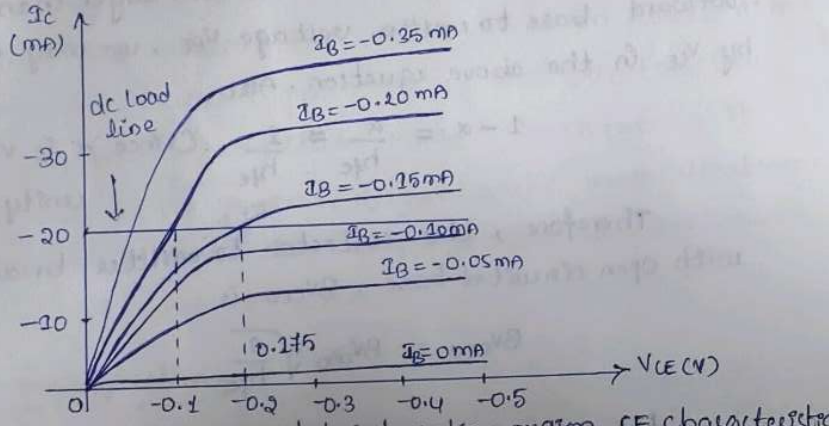
Transistor Switch in Saturation:



(a)



(b) CE characteristics



(c) Expanded saturation region CE characteristics

When a transistor switch is driven from saturation to cut-off, one of the factors which has an important effect on the speed of response is the time required to charge the capacitance which appears in shunt across the output terminals of the transistor. This capacitance must charge through the load resistance R_L, and for this reason, in fast switching circuits, R_L must be kept small. In saturation, the transistor current is nominally V_{cc}/R_L and since R_L is small, it may be

In figure the CB characteristics have been extended into the breakdown region. The curve for $I_E = 0$ is a plot, as a function of V_{CB} of the product of the reverse collector current I_{CO} and the avalanche multiplication factor M. The abrupt growth in I_C as BV_{CBO} is approached is shown along with the slower increase in I_C over the active region that results from the small but not negligible avalanche multiplication.

If a current 'I_E' is caused to flow through the emitter junction, then neglecting the avalanche effect a fraction αI_E reaches the collector junction, where 'α' is the common base current gain. Taking multiplication into account, I_C has the magnitude $M\alpha I_E$. Consequently it appears that in the presence of avalanche multiplication, the transistor behaves as though its common base current gain were α^* where $\alpha^* = M\alpha$

The CE configuration:

Since $h_{fe} = \frac{\alpha}{1-\alpha}$, in the presence of avalanche multiplication, the CE current gain is h^*_{fe}

where $h^*_{fe} = \frac{\alpha^*}{1-\alpha^*} = \frac{M\alpha}{1-M\alpha}$

Now 'α' is a positive number with a maximum magnitude less than unity but $M\alpha$ may equal unity in magnitude at which point h_{fe} becomes infinite. Accordingly

any base current no matter how small, will give rise to an arbitrarily large collector current whenever $M\alpha = 1$. It means breakdown has occured. Therefore whenever the base current is kept fixed, breakdown occurs at the voltage V_{CB} which satisfies the equation

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n} = \frac{1}{\alpha}$$

or breakdown occurs at the voltage V_{CB} given by

$$V_{CB} = BV_{CBO} \sqrt[n]{\frac{1}{h_{fe}}}$$

Since V_{CB} at breakdown is much larger than the small forward base to emitter voltage V_{BE}, we may replace V_{CB} by V_{CE} in the above equation. Also

$$1 - \alpha = \frac{\alpha}{h_{fe}} \approx \frac{1}{h_{fe}}$$ (since α is very close to unity)

Therefore, the collector to emitter breakdown voltage with open circuited base, BV_{CEO} is

$$BV_{CEO} = BV_{CBO} \sqrt[n]{\frac{1}{h_{fe}}}$$

for an n-p-n Ge transistor, a reasonable value for 'n' is 6. If $h_{fe} = 50$, then $BV_{CEO} = BV_{CBO} \sqrt[6]{1/50} = 0.52\, BV_{CBO}$. If $BV_{CEO} = 40\,V$, BV_{CBO} is about half of that i.e about 80 V.

The maximum reverse biasing voltage which may be applied before breakdown between the collector and base terminals of the transistor, under the condition that the emitter lead be open circuited is represented by the symbol BV_{CBO}. This breakdown voltage is a characteristic of the transistor alone. breakdown occurs because of the avalanche multiplication of the current I_{CO} that crosses the collector junction. As a result of this multiplication the current becomes MI_{CO}, in which M is the factor by which the original current I_{CO} is multiplied by the avalanche effect. At a high enough voltage, namely BV_{CBO} the multiplication factor M becomes nominally infinite and the region of breakdown is then attained. Here the current rises abruptly and large changes in current accompany small changes in applied voltage.

The avalanche multiplication factor M depends on the voltage V_{CB} between the collector

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n}$$

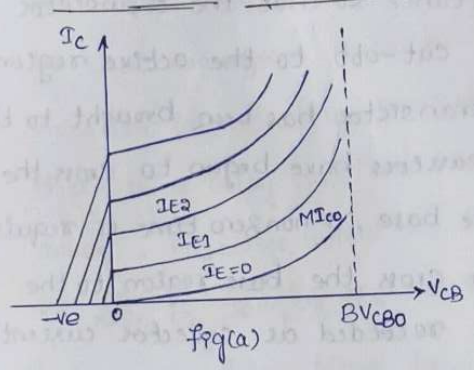
The parameter 'n' lies in the range 2 to 10 and controls the sharpness of the onset of breakdown. when 'n' is large, M continues at nearly unity until V_{CB} approaches very close to BV_{CBO} at which point M soars upwards abruptly. when 'n' is small, the onset of breakdown is gradual.

The collector current increases or decreases along an exponential curve.

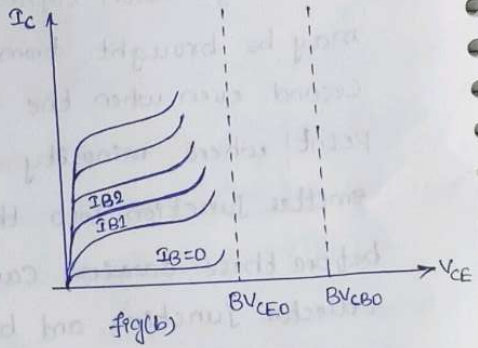
Storage time :

The failure of the transistor to respond to the trailing edge of the driving pulse for the time interval t_s, results from the fact that a transistor in saturation has a saturation charge of excess minority carriers stored in the base. The transistor cannot respond until the saturation excess charge has been removed.

Breakdown voltages of a transistor:



fig(a)



fig(b)

In a transistor switch, the voltage change which occurs at the collector with switching is nominally equal to the collector supply voltage V_{cc}. Since this voltage will be used to operate other circuits and devices, then for the sake of reliability of operation, V_{cc} should be as large as possible. The maximum allowable voltage depends not only on the characteristics of the transistor but also on the associated transistor base circuitry.

when I_c has dropped to 90% of I_{cs} is called the storage time t_s. The storage interval is followed by the fall time t_f, which is the time required for I_c to fall from 90% to 10% of I_{cs}. The turn-off time t_{off} is defined as the sum of storage and fall times i.e "$t_{OFF} = t_s + t_f$".

The delay time:

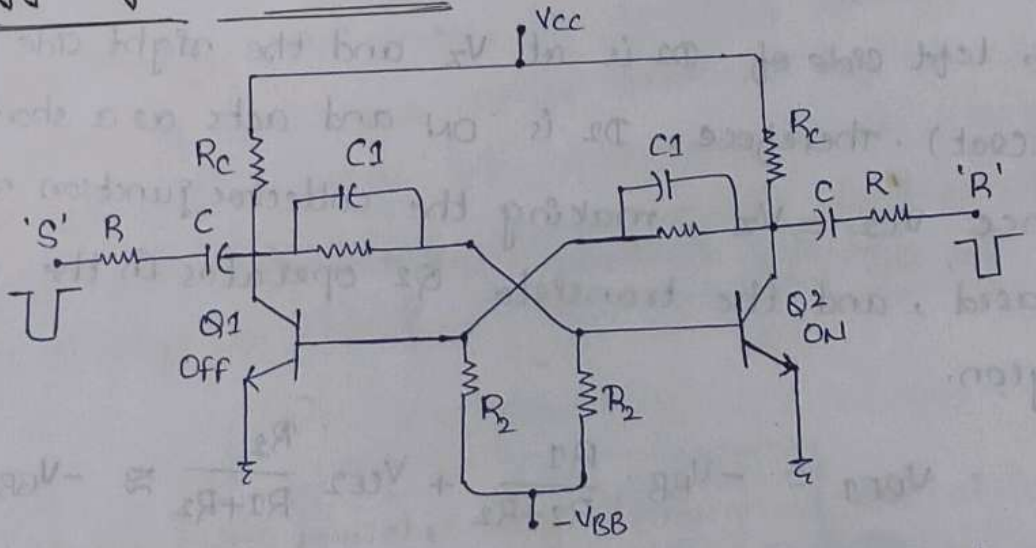
There are 3 factors that contribute to the delay time. First there is a delay which results from the fact that, when the driving signal is applied to the transistor input, a non zero time is required to charge-up the junction capacitance so that the transistor may be brought from cut-off to the active region. Second even when the transistor has been brought to the point where minority carriers have begun to cross the emitter junction into the base, a nonzero time is required before these carriers can cross the base region to the collector junction and be recorded as collector current. Finally, a nonzero time is required before the collector current can rise to 10% of its maximum value.

Rise time and fall time:

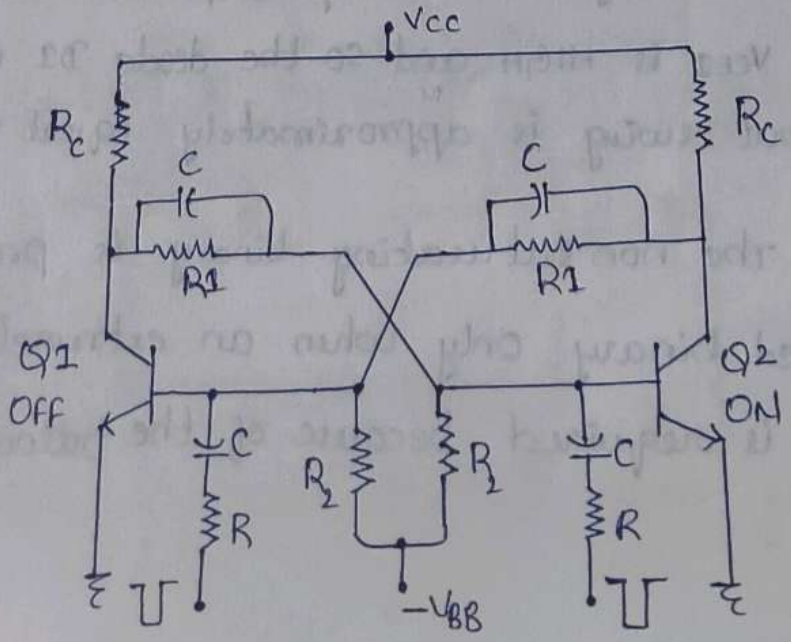
The rise time and fall time are due to the fact that, if a base current step is used to saturate the transistor or to return it from saturation into cut-off, the collector current must traverse the active region.

1. The non-saturating circuits are more complicated than the saturated circuits.
2. The non-saturating circuits consume more power than the saturated circuits.
3. The voltage swing is less stable with temperature, ageing and component replacement than in the case of saturated binary.

Triggering the binary:



(a) Unsymmetrical triggering through a resistor and a capacitor at collectors



(b) At the bases

Figure shows the circuit diagram of non-saturating binary. This is obtained by adding two Zener diodes and two p-n junction diodes to the collector-coupled binary. These diodes ensure that the collector base junctions are reverse biased and hence the transistor is always operating in the active region. Both the Zener diodes D3 and D4 are always biased in the breakdown direction and each has a voltage $V_z < V_{CC}$ across it. The voltage across the diode D1 or D2 is very small in the forward direction. When Q2 is ON, its emitter junction is forward biased with $V_{BE2} \approx 0V$. So the left side of D2 is at V_z and the right side is at $V_{CE(Sat)}$. Therefore, D2 is ON and acts as a short circuit. Hence $V_{C2} = V_z$, making the collector junction reverse biased, and the transistor Q2 operates in the active region.

$$V_{BE1} = -V_{BB} \cdot \frac{R1}{R1+R2} + V_{CE2} \frac{R_2}{R1+R2} \approx -V_{BB} \frac{R1}{R1+R2}$$

This negative voltage keeps Q1 cutoff. With Q1 cutoff, V_{CE1} is HIGH and so the diode D1 is back biased. The output swing is approximately equal to $V_{CC} - V_z$.

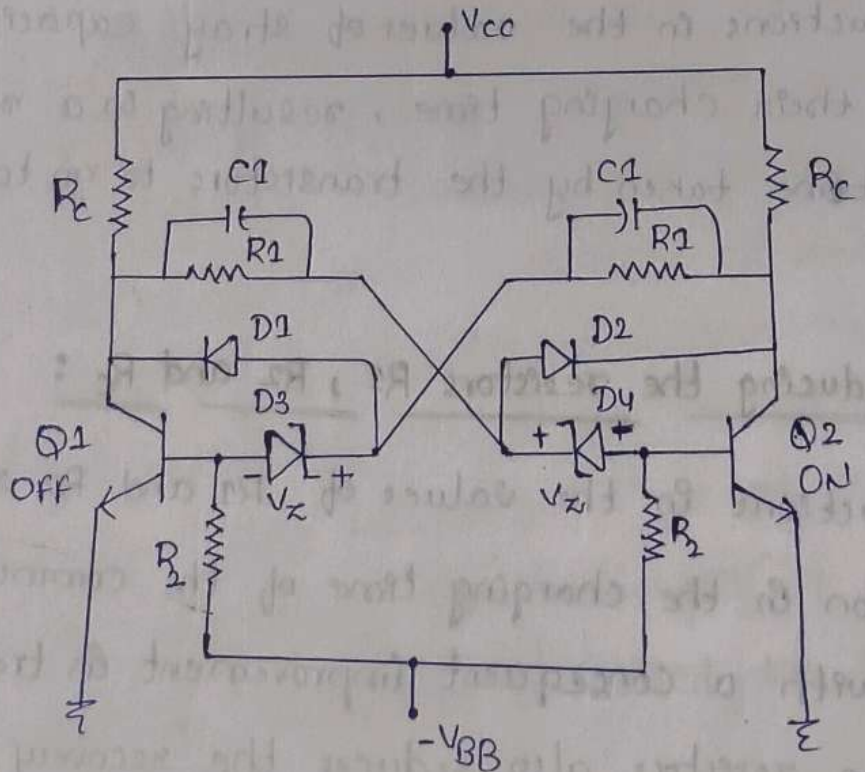
The non saturating binary is preferred over the saturated binary only when an extremely high speed of operation is required because of the following drawbacks.

3. By not allowing the transistors to go into saturation :

When the transistors do not saturate, the storage time will be reduced resulting in fast change from ON to OFF.

Non-Saturated binary :

The binary discussed earlier is a saturated binary. when the transistors are driven into saturation, because of the storage time delay, the speed of operation is reduced. The speed of operation can be increased by not allowing the transistors to go into saturation. Such a binary in which the transistors always operate in the active region only, is called a non saturating binary.



is called the resolution time. If the commutating capacitors are too small, the transition time is increased but the settling time will be small and if the commutating capacitors are too large, the transition time is reduced but the settling time will be large. So, a compromise is called the

The maximum frequency of operation f_{max} is given by

$$f_{max} = \frac{1}{\pi\tau} = \frac{R_1 + R_2}{2R_1R_2C_1}$$

Methods of improving resolution:

The resolution of a binary can be improved by taking the following steps.

1. By reducing all stray capacitances:

Reductions in the values of stray capacitances reduce their charging time, resulting in a reduction in the time taken by the transistors to go to the opposite state.

2. By reducing the resistors R_1, R_2 and R_c:

Reductions in the values of R_1 and R_2 result in a reduction in the charging time of the commutating capacitors with a consequent improvement in transition speed. Reducing resistors also reduces the recovery time.

voltage across C_1 must be 11.3 V and that across C_1' must be 0.3 V. The flipflop would not have settled in its new state until the interchange of voltages had been completed.

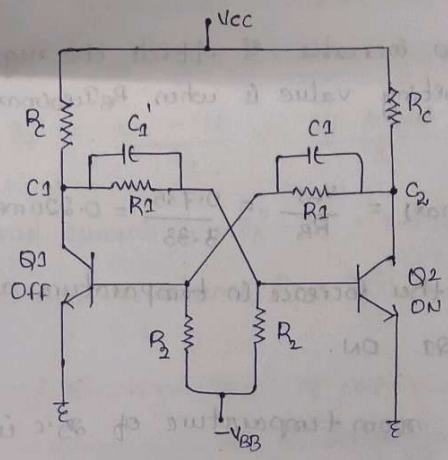
A transistor having been induced to change the state by a triggering signal, a certain minimum time must elapse before a succeeding signal is able to reliably induce the reverse transition. The smallest allowable interval between triggers is called the "resolving time" of the flipflop and its reciprocal is the maximum frequency at which the binary will respond.

The complete transfer of conduction from one device to another involves two phases. The first of these is the transition time during which conduction transfers from one device to another. For this transfer of conduction to take place, the voltages across the input and output capacitances of the transistor have to change. The voltages across the commutating capacitors C_1 and C_1' need not change during this transfer of conduction. After this transfer of conduction, the capacitors are allowed to interchange their voltages. This additional time required for the purpose of completing the recharging of capacitors after the transfer of conduction is called the settling time. The sum of the transition time and the settling time

uncompensated attenuator and so it will have a finite rise time $t_{r1} = (R_1 \| R_2) C_1$. The transition time may be reduced by compensating this attenuator by introducing a small capacitor in parallel with the coupling resistors R1 and R1 of the binary as shown in figure. Since these capacitors are introduced to increase the speed of operation of the device, they are called speed-up capacitors. They are also called transpose or commutating capacitors. So, commutating capacitors are small capacitors connected in parallel with the coupling resistors inorder to increase the speed of operation. The commutating capacitors hasten the removal of charge stored at the base of ON transistor due to minority carriers. If the commutating capacitors are arbitrarily large, the R1-R2 network acts as an overcompensated attenuator and the signal at the collector will be transmitted to the base of the other transistor very rapedly, but large values of capacitors have some disadvantages.

In the flipflop shown in figure, if for example Q1 is OFF and Q2 is ON, the voltages across C1 and C_1' are not alike because, when Q2 is ON and Q1 is OFF, the voltage across C1 is $V_{CE2(sat)} - V_{B1(OFF)}$ which is very small $\simeq 0.3 - (+0) = 0.3\,V$, and the voltage across C_1' must be equal to $V_{CC} - V_{BE2(sat)} \approx 12 - 0.7 = 11.3\,V$. when the circuit is triggered so that Q2 is OFF and Q1 is ON, then the

Commutating capacitors :



We know that the bistable multivibrator has got two stable states and that it can remain in either of its two stable states indefinitely. It can change state only when a triggering signal such as a pulse from some external source is applied. When a triggering signal is applied, conduction has to transfer from one device to another. The transition time is defined as the interval during which conduction transfers from one transistor to another. The reason for this transition time is - even though the input signal is at the base of a transistor may be transferred to the collector with zero rise time the signal at the collector of the transistor cannot be transferred to the base of the other transistor instantaneously. This is because the input capacitance Cq present at the base of the transistor makes the R1 - R2 attenuator acts as an

$$R_B = R_2 \| R_1 = \frac{R_2 R_1}{R_2 + R_1} = \frac{10 \times 5}{10+5} = 3.33 k\Omega$$

when I_{CBO} increases, it offsets the negative bias of Q1 and the limiting value is when $R_B I_{CBO(max)} - V_{B1} = 0$ as shown in fig(b)

$$I_{CBO(max)} = \frac{V_{B1}}{R_B} = \frac{0.735}{3.33} = 0.220 mA = 220 \mu A$$

Any further increase in temparature and hence in I_{CBO} makes Q1 ON.

(d) I_{CBO} at room temparature of 25°C is 10 μA and it doubles for every 10°C rise in temparature.

$$10 \times 2^n = 220 \mu A$$

$$n = \frac{\log 22}{\log 2} = \frac{1.342}{0.3010} = 4.4599$$

(Or)

∴ the maximum temparature at which the device can work properly $= 25 + 10 \times n = 25 + 10 \times 4.4599$

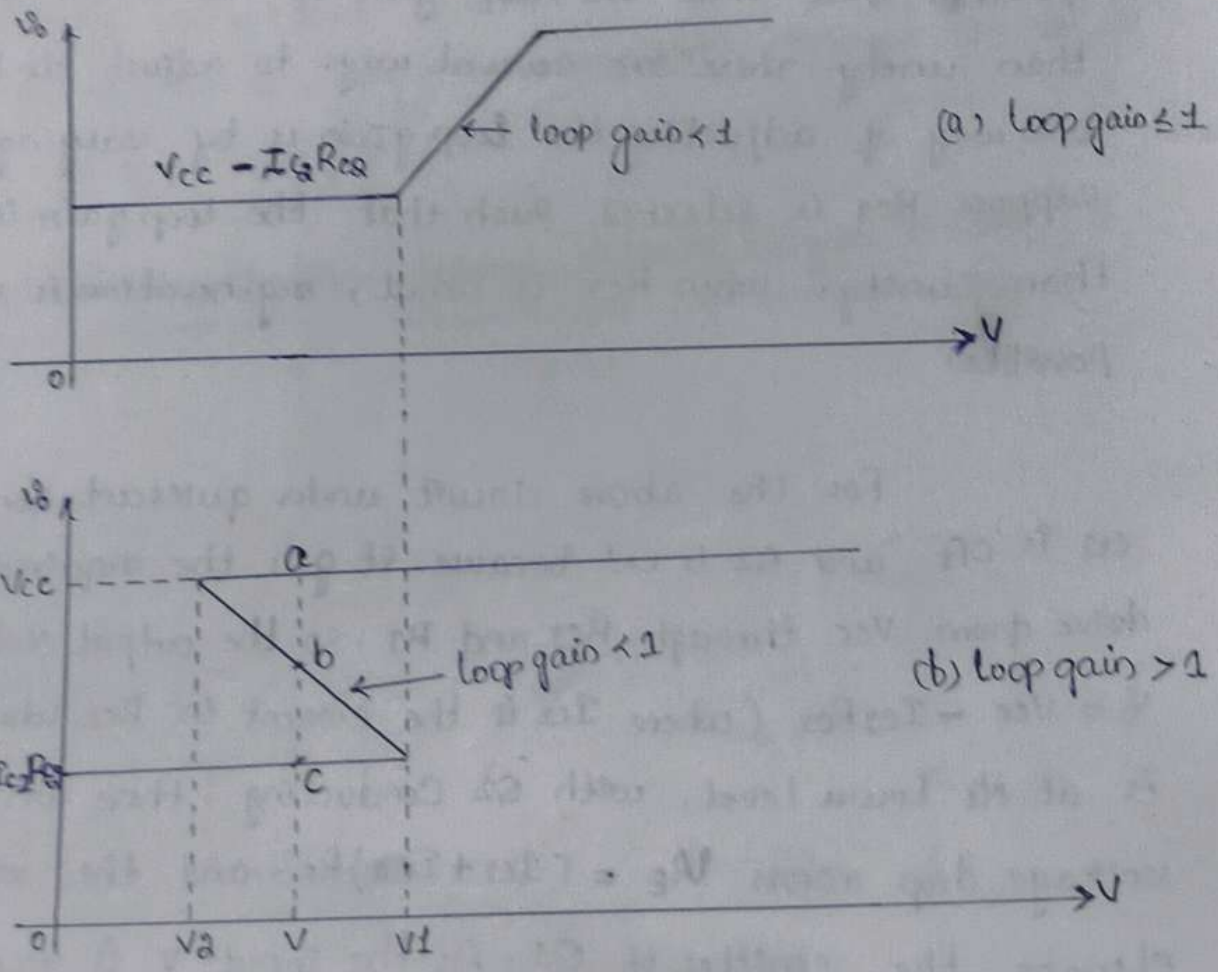
$= 69.599°C$

Figure shows the circuit diagram of an emitter-coupled bistable multivibrator using n-p-n transistors. Quite commonly it is called schmitt trigger after the inventor of its vaccum-tube version. It differs from the basic collector coupled binary in that the coupling from the output of the second stage to the input of the first stage is missing and the feedback is obtained now through a common emitter resistor R_E.

It is a bistable circuit and the existance of only two stable states results from the fact that positive feedback is incorporated into the circuit, and from the further fact that the loop gain of the circuit is greater than unity. There are several ways to adjust the loop gain. One way of adjusting the loop gain is by varying R_{C1}. Suppose R_{C1} is selected such that the loop gain is less than unity. when R_{C1} is small, regeneration is not possible.

For the above circuit under quiescent conditions Q1 is off and Q2 is ON because it gets the required base drive from Vcc through R_{C1} and R_1. So the output voltage $V_0 = V_{cc} - I_{C2}R_{C2}$ (where I_{C2} is the current in R_{C2} when Q1 off) is at its lower level. with Q2 conducting, there will be a voltage drop across $V_E = (I_{C2} + I_{B2})R_E$, and this will elevate the emitter of Q1. As the input 'V' is increased

from zero, the circuit will not respond until Q1 reaches the cut-in point (at $v = V_1$). Until then the output remains at the lower level. With Q1 conducting (for $v > V_1$) until then the output remains at the lower level. With Q1 conducting the circuit will amplify because Q2 is already conducting and since the gain $\Delta V_o / \Delta v$ is positive, the output will rise in response to the rise in input. As 'v' continues to rise, i_{C1} and hence i_{B2} continue to fall and E_2 continues to rise. Therefore a value of v will be reached at which Q2 is turned OFF. At this point $v_o = V_{cc}$ and the output remains constant at this value of V_{cc}, even if the input is further increased.



In fig(a) a plot of v_o versus v is shown for loop gain < 1. Suppose the loop gain is increased by increasing the resistance R_{C2}. Such a change will have negligible effect on the cut-in point V_2 of Q1. However in the region of amplification (i.e for $v > V_2$) the amplifier gain $\Delta v_o / \Delta v$ will increase and so the slope of the rising portion of the plot in fig(a) will be steeper. This increase in slope with increase in loop gain continues until at a loop gain of unity where the circuit has just become regenerative the slope will become infinite. And finally when the loop gain becomes greater than unity, the slope becomes negative and the plot of v_o versus v assumes the 'S' shape shown in fig(b).

The behaviour of the circuit may be described by using this 'S' curve. As 'v' rises from zero voltage, v_o will remain at its lower level ($= V_{cc} - I_{C2} R_{C2}$) until v reaches V_2. (This value of $v = V_2$ at which the transistor Q1 just enters into conduction is called the upper triggering point, UTP) As v exceeds V_2 the output will make an abrupt transition to its higher level ($= V_{cc}$). For $v > V_2$, Q1 is ON and Q2 is OFF. Similarly if 'v' is initially greater than V_2, then as 'v' is decreased, the output will remain at its upper level until 'v' attains a definite level V_1 at which point the circuit makes an abrupt transition to its lower level. For $V < V_1$, Q1 is OFF and Q2 is ON. (This value of $v = V_1$ at which the transistor Q2 resumes conduction)

is called the lower triggering point, LTP). the circuit exhibits hysteresis, that is, to effect a transition in one direction we must drive past beyond the voltage at which the reverse transition took place.

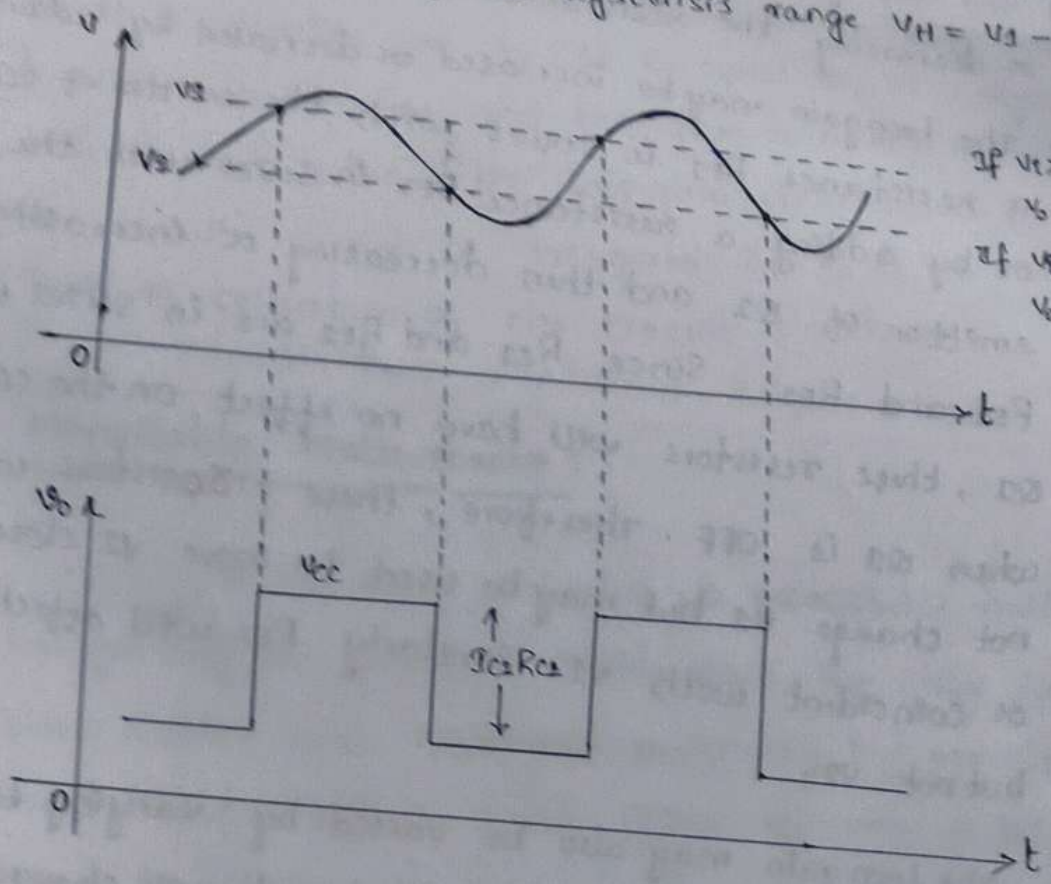
A vertical line drawn at $v = V$ which lies b/w v_2 and v_1 intersects the curve at three points a, b and c. the upper and lower points a and c are points of stable equilibrium. the 'S' curve is a plot of values which satisfy Kirchhoff's laws and which are consistent with the transistor characteristics. at $v = V$, the circuit will be at 'a' or 'c', depending on the direction of approach of v towards V. when $v = V$ in the range between v_2 and v_1, the schmitt circuit is in one of its two possible stable states and hence is a bistable circuit.

Applications of schmitt trigger:

A most important application of the schmitt trigger is its use as an amplitude comparator to mark the instant at which an arbitrary waveform attains a particular reference level. As input v rises to v_1 or falls to v_2, the circuit makes a fast regenerative transfer to the other state.

Another important application of the schmitt trigger is as a squaring circuit. It can convert a sinusoi

into a square wave. Infact, any slowly varying input waveform can be converted into a square wave with faster leading and trailing edges as shown in figure below, if the input has large enough excursions to carry the input beyond the limits of the hysteresis range $V_H = V_1 - V_2$



Hysteresis :

If the amplitude of the periodic input signal is large compared with the hysteresis range V_H, then the hysteresis of the schmitt trigger is not a matter of concern. In some applications, a large hysteresis range will not allow the circuit to function properly.

Hysteresis may be eliminated by adjusting the loop gain of the circuit to unity. Such an adjustment may be made in a number of ways.

1. The loop gain may be increased or decreased by increasing or decreasing the resistance R_{E1}.

2. The loop gain may be increased or decreased by adding a resistance R_{E1} in series with the emitter of Q1, or by adding a resistance R_{E2} in series with the emitter of Q2 and then decreasing or increasing R_{E1} and R_{E2}. Since R_{E1} and R_{E1} are in series with Q1, these resistors will have no effect on the circuit when Q1 is OFF. Therefore, these resistors will not change V_1 but may be used to move V_2 closer to or coincident with V_1. Similarly R_{E2} will affect V_1 but not V_2.

3. The loop gain may also be varied by varying the ratio R_1/R_1+R_2. Such an adjustment will change both V_1 and V_2.

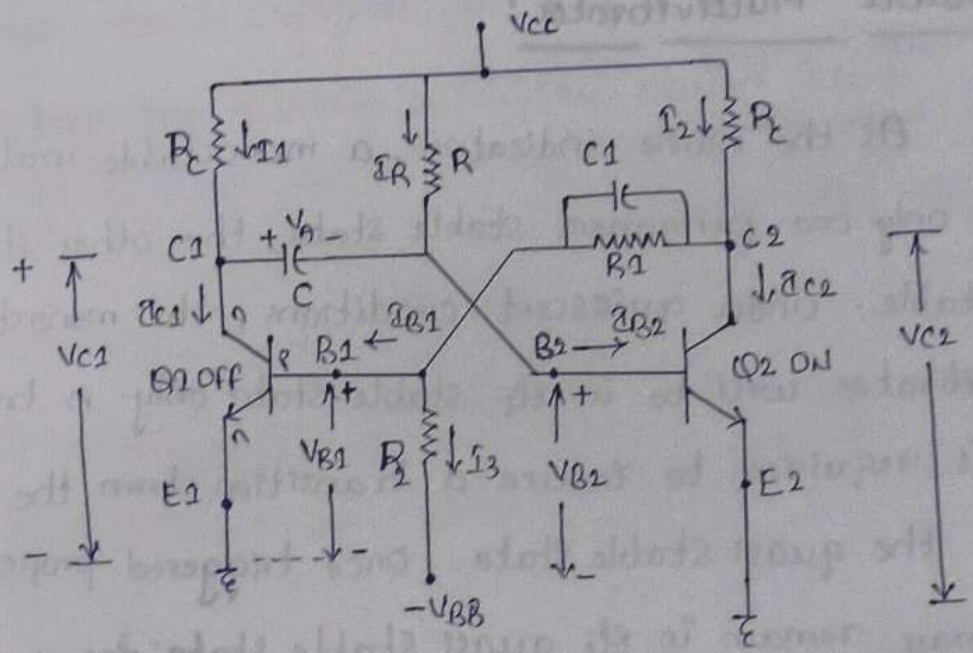
4. The loop gain may be increased by increasing the values of R_3.

If R_{E1} and R_{E2} is larger than the value required to give zero hysterisis, then the gain will be less than unity and the circuit will not change state.

element is a capacitor.

When triggered, since the circuit returns to its original state by itself after a time T, it is known as a one shot, a single-step, or a univibrator. Since it generates a rectangular waveform which can be used to gate other circuits, it is also called a gating circuit. Since it generates a fast transition at a predetermined time T after the input trigger, it is also referred to as a delay circuit.

The collector coupled monostable multivibrator :



The collector coupled monostable multivibrator is shown in the above figure. The collector of Q2 is coupled to the base of Q1 by a resistor R (dc coupling). C1 is the commutating capacitor introduced to increase the speed of operation. The base of Q1 is connected to $-V_{BB}$ through a

resistor R_2, to ensure that Q_1 is cutoff under quiescent conditions. In fact, B may be returned to even a small positive voltage but connecting it to V_{cc} is advantageous.

The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q_2 ON (i.e in saturation) and Q_1 OFF (i.e in cut-off). The multivibrator may be induced to make a transition out of its state by the application of a negative trigger at the base of Q_2 or at the collector of Q_1. Since triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed.

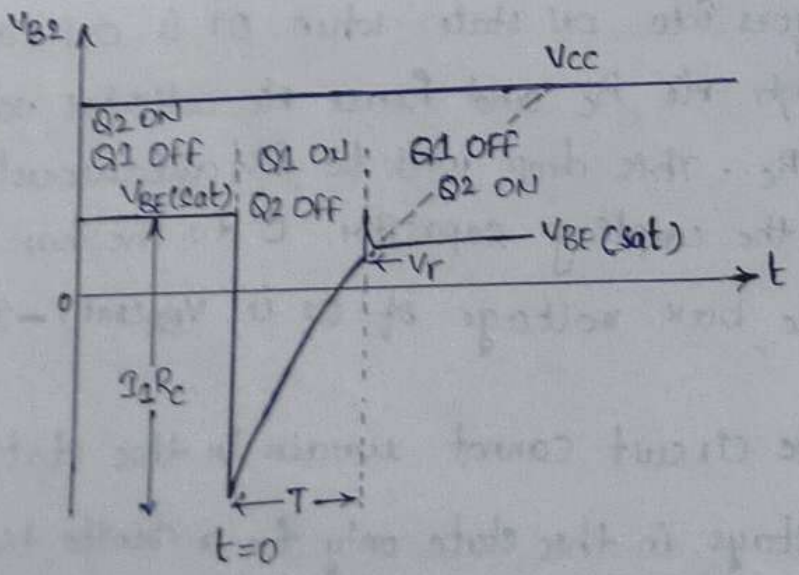
When a negative signal is applied at the base of Q_2 at $t=0$, due to regenerative action Q_2 goes into OFF state and Q_1 goes into ON state. When Q_1 is ON, a current I_1 flows through its R_C and hence its collector voltage drops suddenly by $I_1 R_C$. This drop will be instantaneously transmitted through the coupling capacitor 'C' to the base of Q_2. So at $t = 0^+$, the base voltage of Q_2 is $V_{BE(sat)} - I_1 R_C$.

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time T) because when Q_1 conducts, the coupling capacitor 'C' charges from V_{cc} through the conducting transistor Q_1 and hence the potential at the base of Q_2 rises exponentially with a time constant $(R+R_0)C \approx RC$, where R_0 is the conducting

transistor output impedance including the resistance R_C. when it passes the cut-in voltage V_γ of Q2 (at time $t=T$), a regenerative action takes place turning Q1 OFF and eventually returning the multivibrator to its initial stable state.

The transition from the stable state to the quasi stable state takes place at $t=0$, and the reverse transition from the quasi-stable state to the stable state takes place at $t=T$. The time T for which the circuit is in its quasi-stable state is also referred to as the delay time and also as the gate width, pulse width or pulse duration. The delay time may be varied by varying the time constant $\tau (=RC)$.

Expression for the gate width 'T' of a monostable multivibrator neglecting the reverse saturation current I_{CBO}:



(a) Voltage variation at the base of Q2 during the quasi-stable state (neglecting I_{CBO})

Figure shows the waveform at the base of transistor Q2 of the monostable multivibrator.

For $t<0$, Q2 is ON and so $V_{B2} = V_{BE(sat)}$. At $t=0$, a negative signal applied brings Q2 to OFF state and Q1 into saturation. A current I_1 flows through R_C of Q1 and hence V_{C1} drops abruptly by I_1R_C volts and so V_{B2} also drops by I_1R_C instantaneously. So at $t=0$, $V_{B2} = V_{BE(sat)} - I_1R_C$. For $t>0$ the capacitor charges with a time constant RC, and hence the base voltage of Q2 rises exponentially towards V_{CC} with the same time constant RC, and hence the base voltage of Q2 rises exponentially towards V_{CC} with the same time constant. At $t=T$, when this base voltage rises to the cut-in voltage level V_γ of the transistor, Q2 goes to ON state, and Q1 to OFF state and the pulse ends.

In the interval $0<t<T$, the base voltage of Q2, i.e V_{B2} is given by

$$V_0 = V_f - [V_f - V_{in}]e^{-t/\tau}$$

$$V_{B2} = V_{CC} - \{V_{BB} - [V_{BE(sat)} - I_1R_C]\} e^{-t/\tau}$$

But $I_1R_C = V_{CC} - V_{CE(sat)}$ {because at $t=0^-$, $V_{C1} = V_{CC}$ and at $t=0^+$, $V_{C1} = V_{CE(sat)}$}

$$V_{B2} = V_{CC} - \left[V_{CC} - \{V_{BE(sat)} - (V_{CC} - V_{CE(sat)})\}\right] e^{-t/\tau}$$

$$= V_{CC} - \left[2V_{CC} - \{V_{BE(sat)} + V_{CE(sat)}\}\right] e^{-t/\tau}$$

At $t=T$, $V_{B2} = V_\gamma$

$$V_f = V_{cc} - [2V_{cc} - \{V_{CE(sat)} + V_{BE(sat)}\}]\, e^{-T/\tau}$$

$$i.e \quad e^{T/\tau} = \frac{2V_{cc} - [V_{CE(sat)} + V_{BE(sat)}]}{V_{cc} - V_f}$$

$$T/\tau = \frac{\ln\left[2\left(V_{cc} - \frac{\{V_{CE(sat)} + V_{BE(sat)}\}}{2}\right)\right]}{V_{cc} - V_f}$$

$$i.e \quad T = \tau \ln 2 + \tau \ln \frac{V_{cc} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2}}{V_{cc} - V_f}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction voltages for either Ge or Si transistors i.e

$$V_f = \frac{V_{CE(sat)} + V_{BE(sat)}}{2}$$

$\therefore$ Neglecting the second term in the expression for T

$$T = \tau \ln 2$$

$$i.e \quad T = (R + R_o) C \ln 2 = 0.693 [R + R_o] C$$

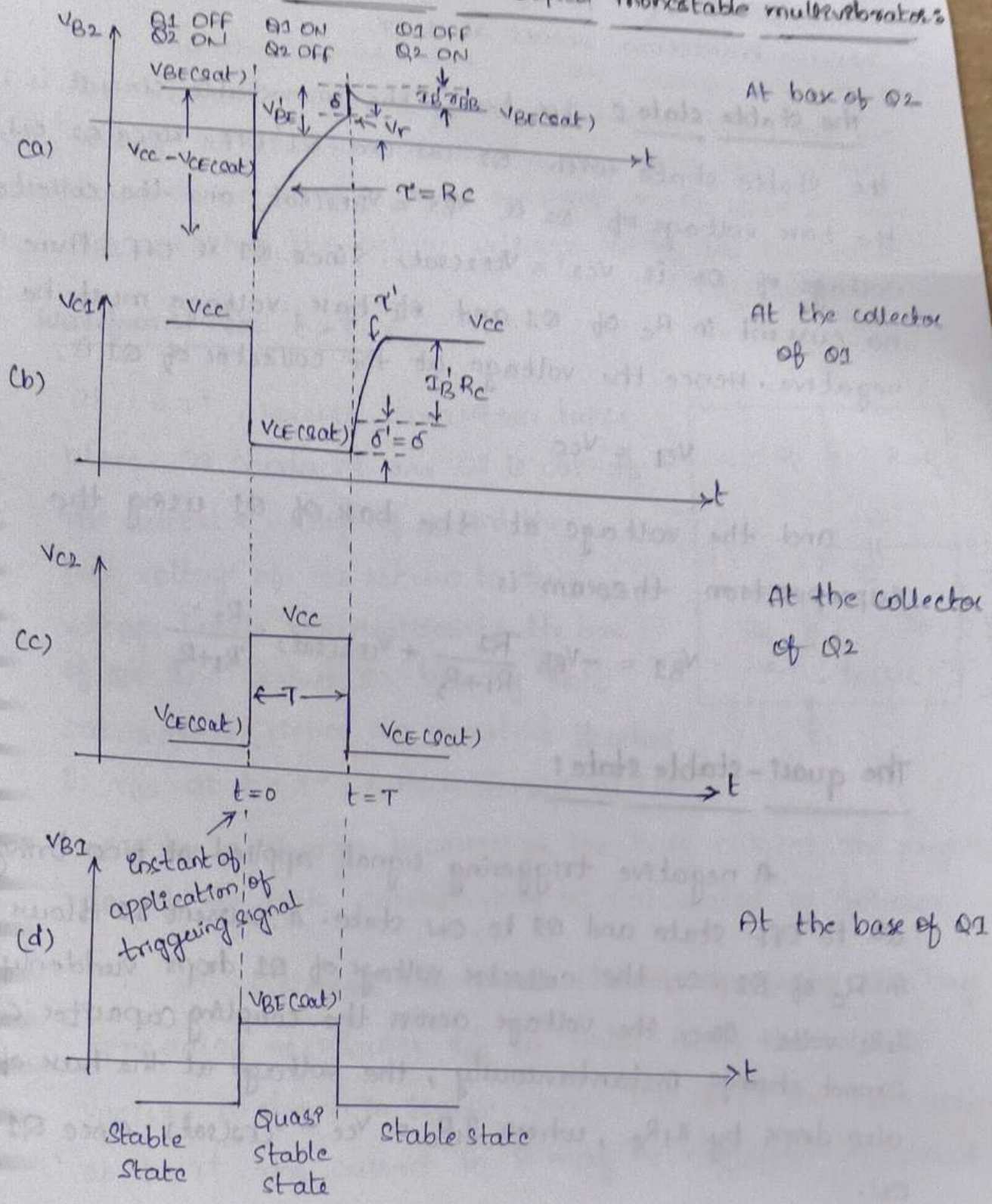
but for a transistor in saturation $R_o \ll R$

Gate width, $T = 0.693 RC$

The larger the V_{cc} is, compared to the saturation junction voltages, the more accurate the result is.

The gate width can be made very stable (almost independent of transistor characteristics, supply voltages and resistance values) if Q1 is driven into saturation during the quasi stable state.

Waveforms of the collector-coupled monostable multivibrator



waveforms at the collectors and bases of the collector-coupled monostable multivibrator.

The triggering signal is applied at $t=0$, and the reverse transition occurs at $t=T$.

The stable state: For $t<0$, the monostable circuit is in its stable state with Q2 ON and Q1 OFF. Since Q2 ON, the base voltage of Q2 is $V_{B2} = V_{BE2(sat)}$ and the collector voltage of Q2 is $V_{C2} = V_{CE2(sat)}$. Since Q1 is OFF, there is no current in R_C of Q1 and its base voltage must be negative. Hence the voltage at the collector of Q1 is,

$$V_{C1} = V_{CC}$$

and the voltage at the base of Q1 using the superposition theorem is

$$V_{B1} = -V_{BB}\frac{R1}{R_1+R_2} + V_{CE2(sat)}\cdot\frac{R_2}{R_1+R_2}$$

The quasi-stable state:

A negative triggering signal applied at $t=0$ brings Q2 to OFF state and Q1 to ON state. A current I1 flows in R_C of Q1. So, the collector voltage of Q1 drops suddenly by I_1R_C volts. Since the voltage across the coupling capacitor 'C' cannot change instantaneously, the voltage at the base of Q2 also drops by I_1R_C, where $I_1R_C = V_{CC} - V_{CE2(sat)}$. Since Q1 is ON.

$$V_{B1} = V_{BE1(sat)} \quad \text{and} \quad V_{C1} = V_{CE1(sat)}$$

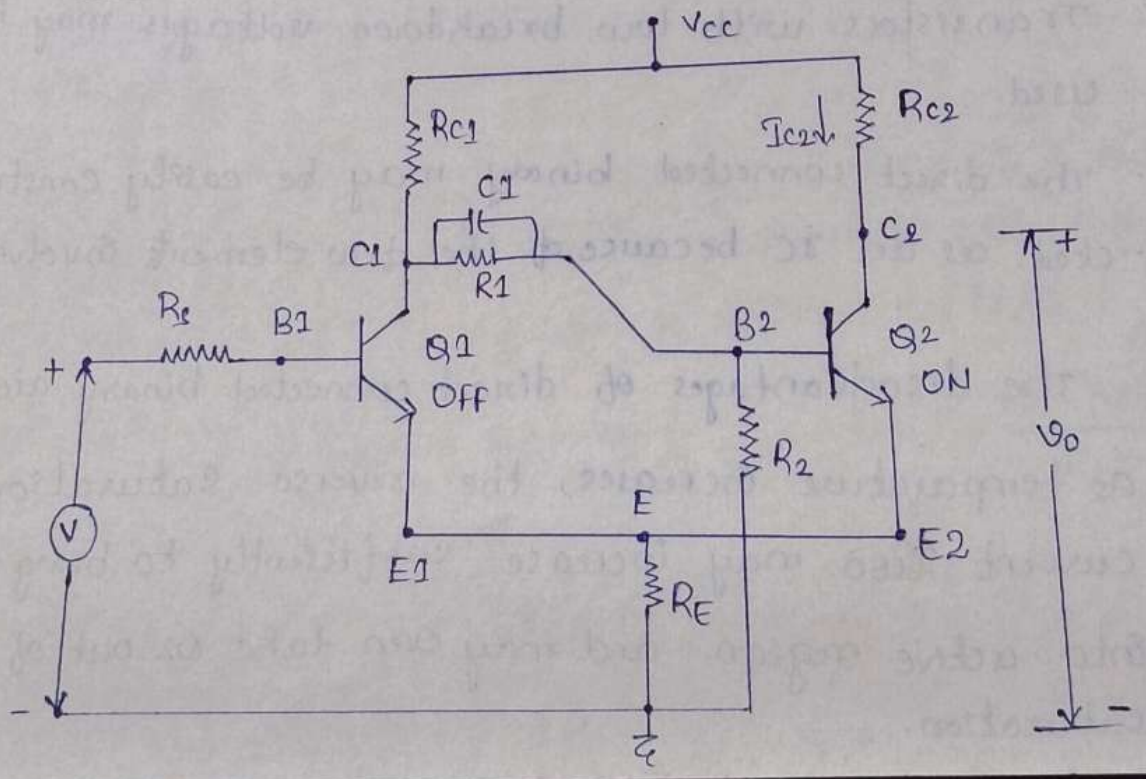
2. Since Q_2 is driven heavily into saturation, the storage time delay will be large and the switching speed will be low.

3. The output voltages are equal to their saturation base and collector voltages, and these parameters may vary appreciably from transistor to transistor.

4. The voltage swing is only a fraction of a volt and hence the binary is susceptible to spurious voltages.

5. Since an OFF collector is tied directly to an ON base, it is difficult to trigger the binary by the usual method of applying a pulse to the OFF transistor. To supply sufficient current to take the ON transistor out of saturation, an amplified trigger circuit is usually required.

The emitter-coupled binary [schmitt trigger circuit]:



and hence Q1 is driven heavily into saturation. So for a Ge transistor, $V_{CE1} = 0.05$ V and $V_{BE1} = 0.3$ V Because of the direction connection between the collector of Q1 and the base of Q2, $V_{BE2} = V_{CE1} = 0.05$ V, a small positive value. So Q2 is not off and it will be conducting slightly. The output swing $= V_{CE2} - V_{CE1} = V_{BE1} - V_{CE1} = 0.3 - 0.05 =$ 0.25 V. Even-though it has some advantages, there are many serious disadvantages too, and so this circuit is not used these days. It was available in IC form as DCTL earlier.

The advantages of direct connected binary are

1. Its extreme simplicity.
2. Only one supply voltage of low value about 1.5 V is required.
3. Low power dissipitation.
4. Transistors with low breakdown voltages may be used.
5. The direct connected binary may be easily constru-cted as an IC because of the few elements involved.

The disadvantages of direct connected binary are

1. As temparature increases, the reverse saturation current I_{CBO} may increase sufficiently to bring Q1 into active region and may even take Q2 out of saturation.

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A direct connected binary:

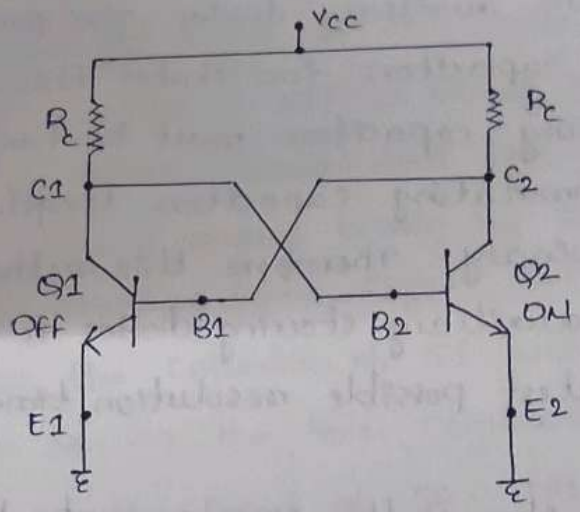


Figure shows a direct connected binary. No coupling elements are used and the collector of each transistor is connected to the base of the other transistor directly by a wire. In one stable state, transistor Q1 is in saturation and Q2 is conducting slightly, and in the other stable state Q2 is in saturation and Q1 is conducting slightly.

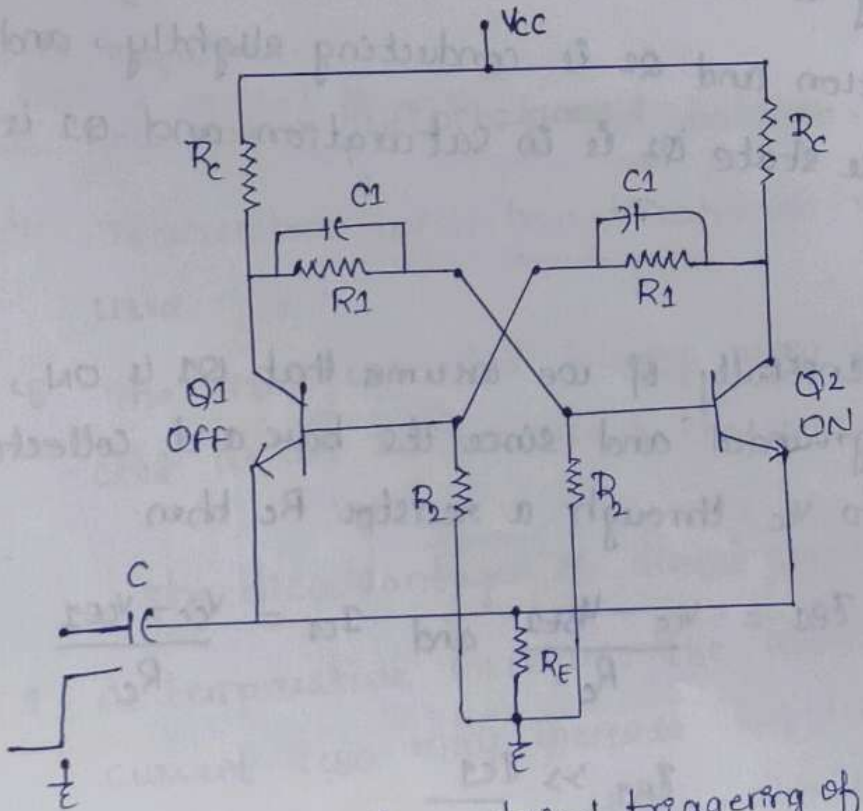
Initially if we assume that Q1 is ON, since its emitter is grounded and since its base and collector are connected to V_{cc} through a resistor R_c then

$$I_{B1} = \frac{V_{cc} - V_{BE1}}{R_c} \quad \text{and} \quad I_{C1} = \frac{V_{cc} - V_{CE1}}{R_c}$$

$$I_{B1} >> \frac{I_{C1}}{h_{fe}}$$

Triggering may also be done symmetrically without the use of the auxiliary diodes. The presence of commutating capacitors facilitates this, but for this, the commutating capacitors must be large and large values of commutating capacitors lengthen the settling time of the binary. Therefore this method of triggering without the auxiliary steering diodes is not employed where the shortest possible resolution time is required.

figure) shows the arrangement for triggering a self-biased bistable multivibrator without steering diodes. Here a positive step is applied at the common emitters of the flipflop.

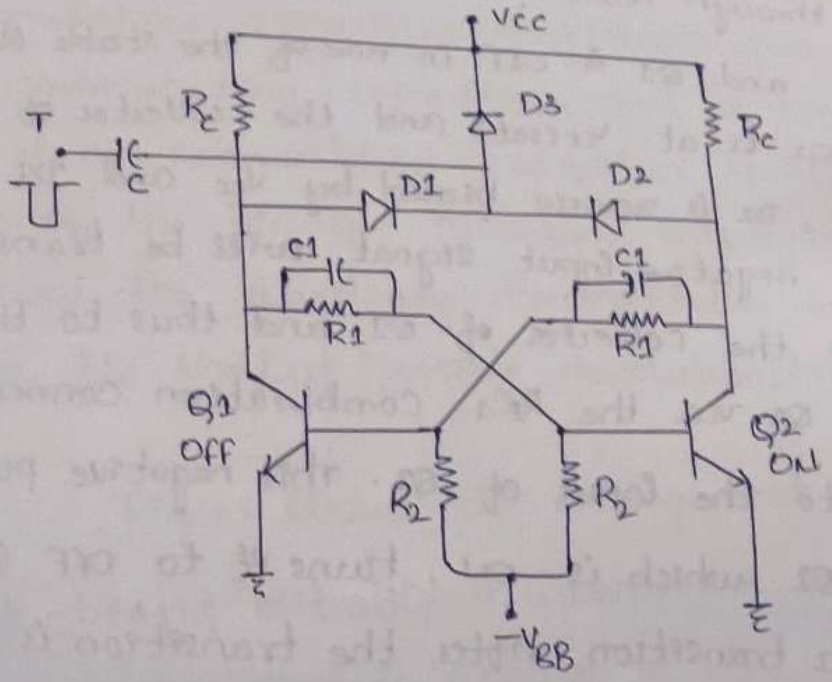


(c) Symmetrical triggering of self-biased binary

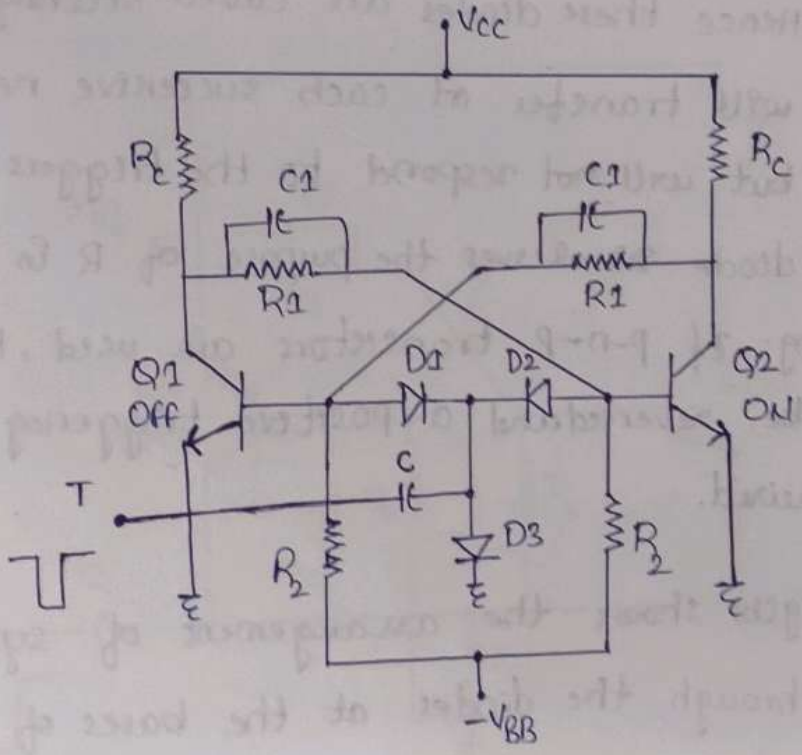
Fig(a) shows an arrangement for symmetrical triggering through diodes at the collectors of the transistors. If Q2 is ON and Q1 is OFF in one of the stable states, the collector of Q2 is at $V_{CE(sat)}$ and the collector of Q1 is at V_{CC}. Therefore, D2 is reverse biased by V_{CC} and D1 is at zero bias. Hence a negative input signal will be transmitted through D1 to the collector of Q1 and thus to the base of the ON stage Q2 via the R_1C_1 combination connecting the output of Q1 to the input of Q2. This negative pulse at the base of Q2 which is ON, turns it to OFF state thus causing a transition. After the transition is completed D1 will be reverse biased and D2 will be at zero bias. So the next negative pulse will pass through D2 instead of through D1. Hence these diodes are called steering diodes. The binary will transfer at each successive negative input pulse or step but will not respond to the triggers of opposite polarity. The diode D3 serves the purpose of R in unsymmetrical triggering. If p-n-p transistors are used, then the diodes must be reversed and a positive triggering signal would be required.

Fig(b) shows the arrangement of symmetrical triggering through the diodes at the bases of the transistors.

Triggering symmetrically through a unilateral device :

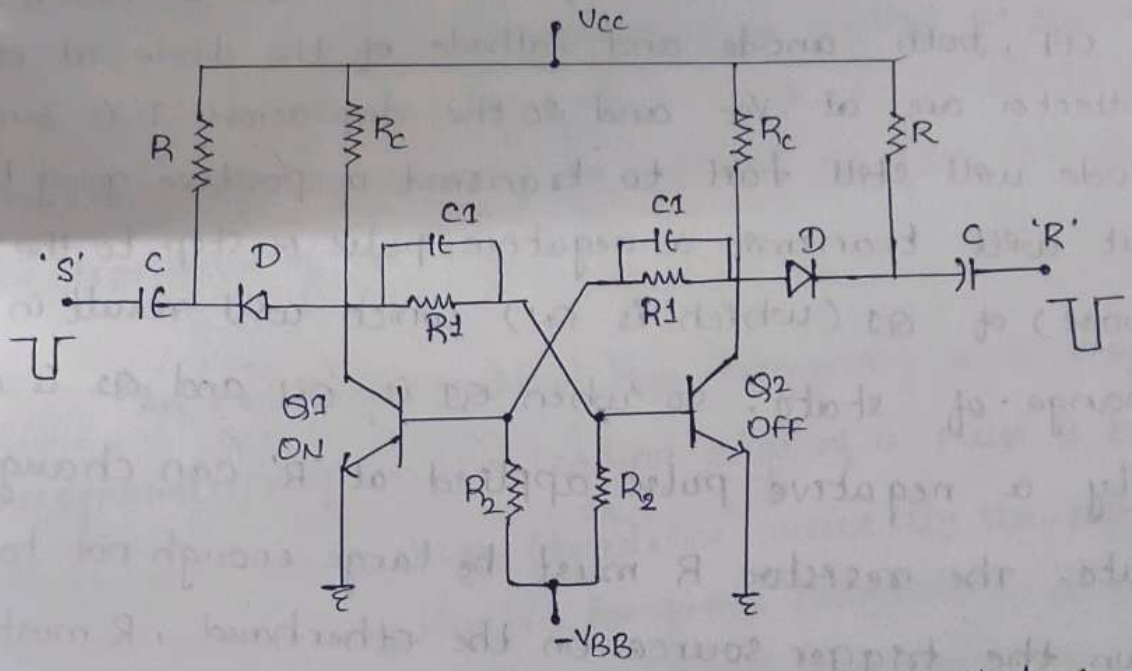


(a) symmetrical triggering through diodes at collector

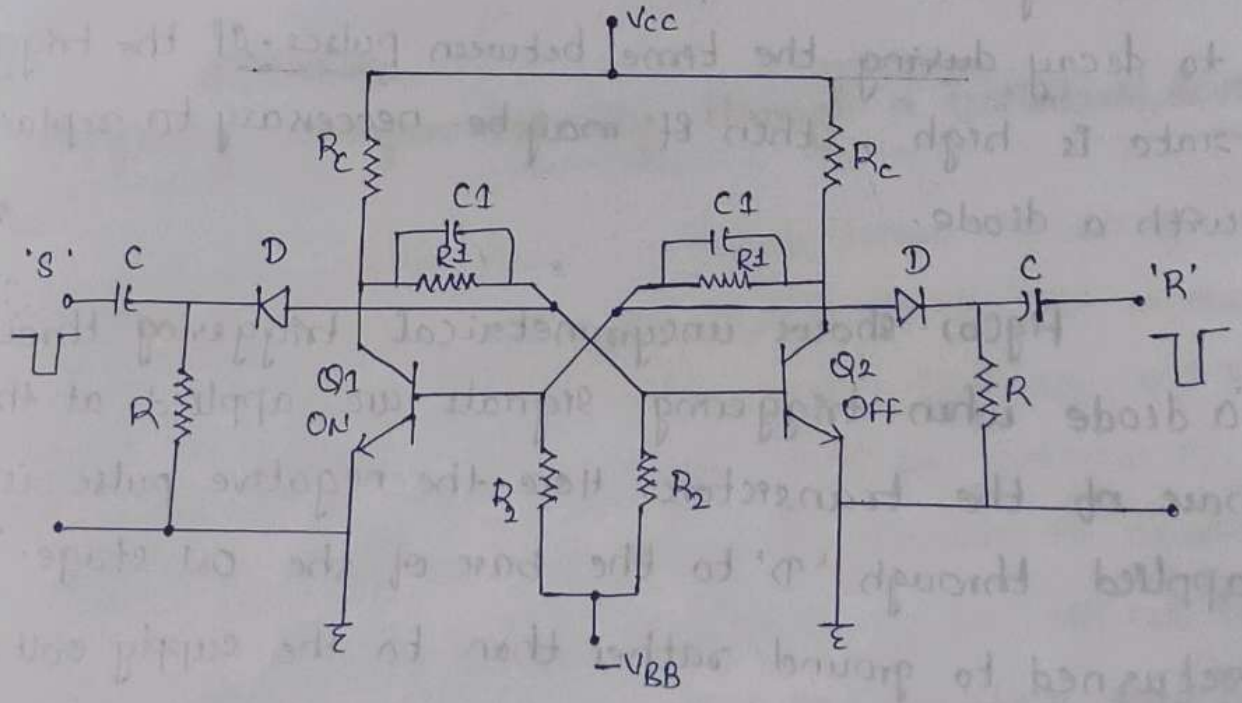


(b) symmetrical triggering through diodes at bases

et to the flipflop. In this case a diode need not be used because the amplifier can provide the unilateral action previously supplied by the diode.



(a) Unsymmetrical triggering at collectors.



(b) Unsymmetrical triggering at base

transmitted unless it has an amplitude larger than this voltage drop which anyway cannot effect the state of Q2. so no change of state can take place by the application of a pulse at the collector of Q1 when Q1 is ON. when Q2 is off, both anode and cathode of the diode at its collector are at Vcc and so the drop across 'D' is zero bias. The diode will still fail to transmit a positive going trigger, but will transmit a negative pulse or step to the input (base) of Q1 (which is ON) which will result in a change of state. so when Q1 is ON and Q2 is OFF, only a negative pulse applied at 'R' can change the state. The resistor R must be large enough not to load down the trigger source. on the other hand, R must be small enough so that any charge which accumulates on 'C' during the interval when 'D' conducts will have time to decay during the time between pulses. If the triggering rate is high, then it may be neccessary to replace R with a diode.

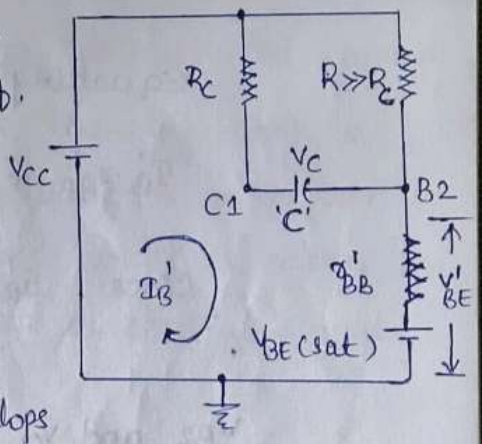
fig(b) shows unsymmetrical triggering through a diode when triggering signals are applied at the base of the transistors. Here the negative pulse is applied through 'D' to the base of the ON stage. 'R' is returned to ground rather than to the supply voltage. If the trigger amplitude available is small, it may be neccessary to amplify the signal before applying

Also $V_{B2} = V_{BE2}(sat) - I_1 R_C$ and $V_{C2} = V_{CC}\frac{R_1}{R_1+R_C} + V_{BE1}(sat)\frac{R_C}{R_1+R_C}$

In the interval $0 < t < T$, the voltages V_{C1}, V_{B1} and V_{C2} remain constant at their values at $t=0$, but the voltage at the base of Q2 i.e V_{B2} rises exponentially towards V_{CC} with a time constant, $\tau = RC$ until at $t=T$, V_{B2} reaches the cut-in voltage V_γ of the transistor.

Waveforms for $t > T$:

At $t = T^+$, reverse transition takes place. Q2 conducts and Q1 is cut-off. The collector voltage of Q2 and the base voltage of Q1 return to their voltage levels transmitted to the base of Q2 and drives Q2 heavily into saturation. Hence an overshoot develops in V_{B2} at $t = T^+$, which decays as the capacitor recharges because of the base current. The magnitude of the base current may be calculated as follows.



Replace the input circuit of Q2 by the base spreading resistance r'_{BB} in series with the voltage $V_{BE}(sat)$ as shown in figure above. Let I'_B be the base current at $t = T^+$. The current in R may be neglected compared to I'_B.

$$V'_{BE} = I'_B R'_{BB} + V_{BE}(sat) \quad \text{and} \quad V_C = V_{CC} - I'_B R_C - V'_{BE}$$

The jumps in voltages at B2 and C1 are respectively, given by

$$\delta = V'_{BE} - V_r = I'_B r'_{BB} + V_{BE(sat)} - V_r \quad \text{and}$$

$$\delta' = V_{CC} - V_{CE(sat)} - I'_B R_C$$

Since C1 and B2 are connected by a capacitor 'C' and since the voltage across the capacitor cannot change instantaneously, these two discontinuous voltage changes δ and δ' must be equal.

Equating them,

$$I'_B r'_{BB} + V_{BE(sat)} - V_r = V_{CC} - V_{CE(sat)} - I'_B R_C$$

$$\text{Since} \quad I'_B = \frac{V_{CC} - V_{BE(sat)} - V_{CE(sat)} + V_r}{R_C + r'_{BB}}$$

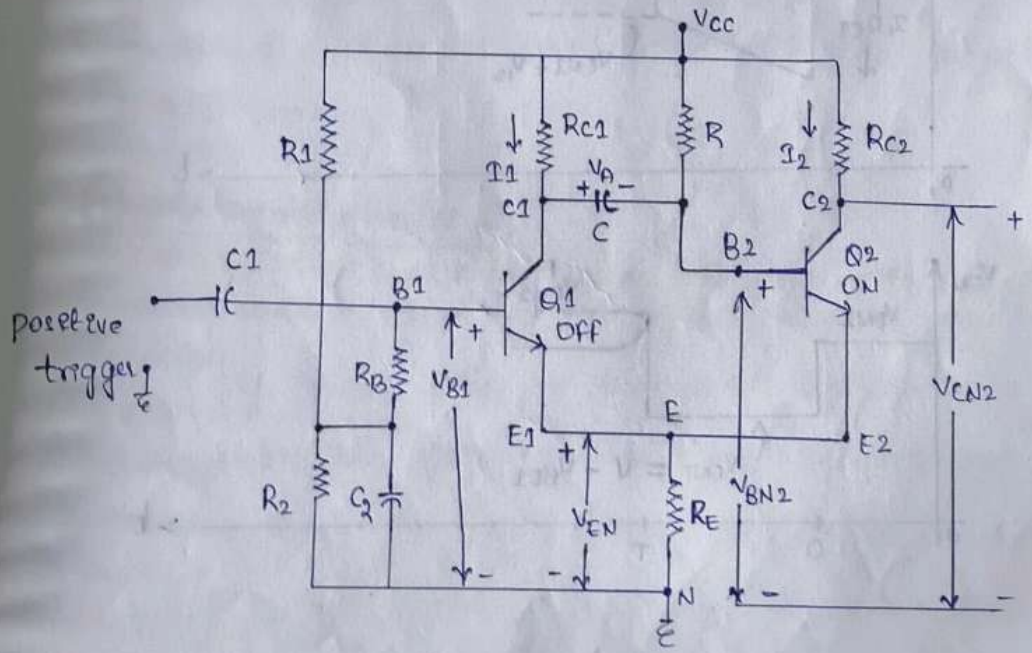
V_{B2} and V_{C1} decay to their steady state values with a time constant

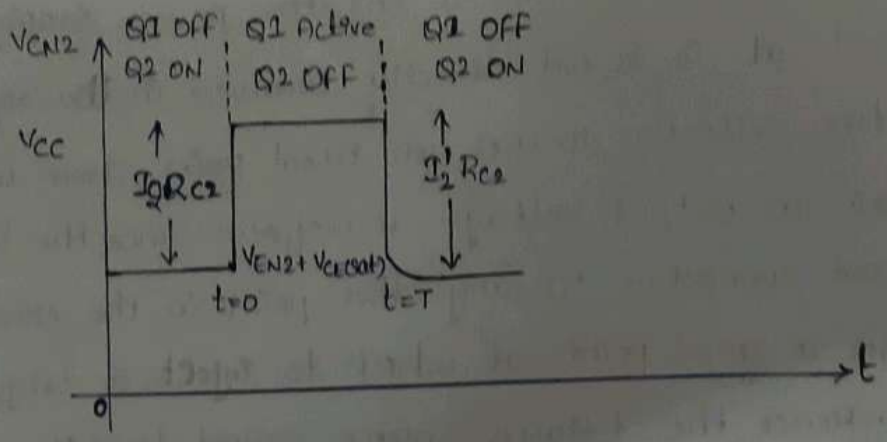
$$\tau' = (R_C + r'_{BB})\, C$$

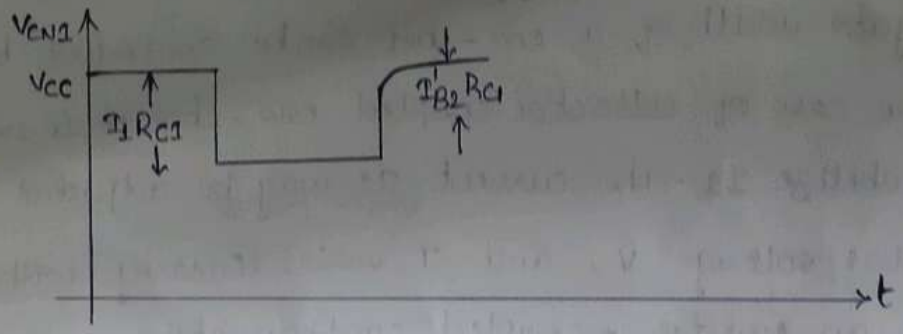
The emitter coupled monostable multivibrator :

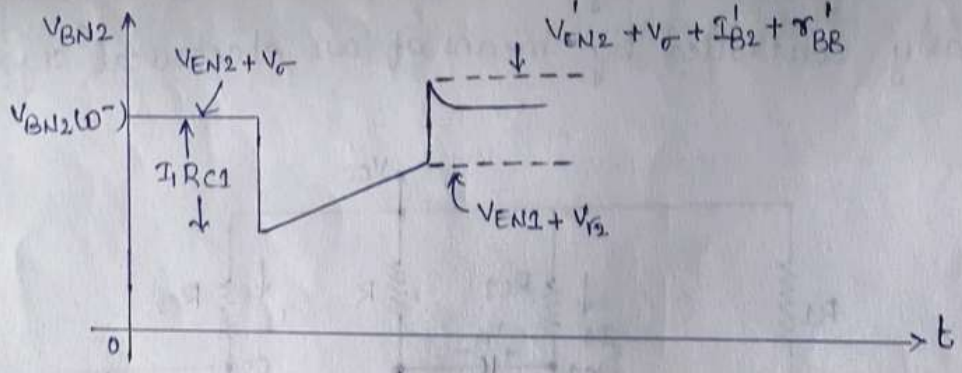
Figure shows the circuit diagram of an emitter-coupled monostable multivibrator. It differs from the collector coupled one shot in that the collector of Q2 is not coupled to the base of Q1 and instead the feedback has been provided through a common emitter resistance R_E.

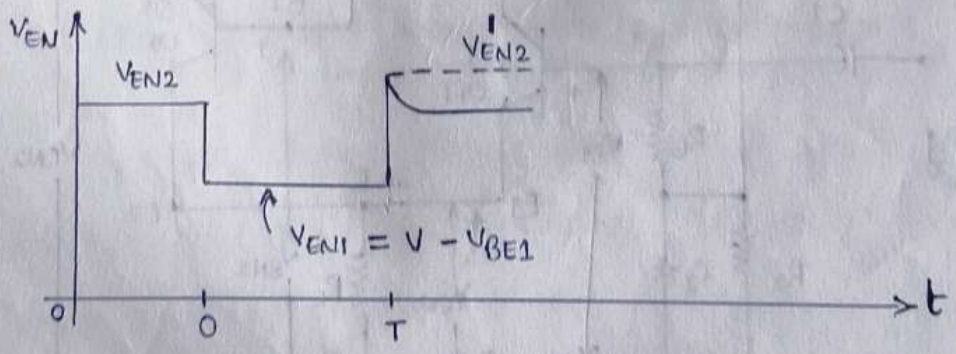
Also there is no need for a negative power supply. Since the signal at C_2 is not directly involved in the regenerative loop, this collector makes an ideal point from which to obtain an output voltage waveform. Since the base of Q1 is not connected to any other point in the circuit, it makes a good point at which to inject a triggering signal. Hence the trigger source cannot load the circuit. The gate width of a one-shot can be controlled through I_1. In the case of collector coupled one-shot it is not possible to stabilize I_1. The current I_1 may be adjusted through the bias voltage V, and T varies linearly with V. Hence an emitter-coupled configuration makes an excellent gate wave generator whose width is easily and linearly controlled by means of an electrical signal.




V_{CN2}
Q1 OFF
Q2 ON
Q1 Active
Q2 OFF
Q1 OFF
Q2 ON
V_{CC}
$I_2 R_{C2}$
$I_2' R_{C2}$
$V_{EN2} + V_{CE(sat)}$
t=0
t=T
t
0


V_{EN1}
V_{CC}
$I_1 R_{C1}$
$I_{B2}' R_{C1}$
t


V_{BN2}
$V_{EN2} + V_\sigma$
$V_{BN2}(0^-)$
$I_1 R_{C1}$
$V_{EN2}' + V_\sigma + I_{B2}' + r_{BB}'$
$V_{EN1} + V_{\gamma 2}$
0
t


V_{EN}
V_{EN2}
V_{EN2}'
$V_{EN1} = V - V_{BE1}$
0
0
T
t

In the stable state, Q2 is ON because it gets the required base drive from V_{CC} through R and develops a potential V_{EN} across the resistor R_E. The biasing resistors R1 and R2 are selected such that V_{B1} is smaller than V_{EN} to ensure that Q1 is OFF. This is the stable state. when a positive going triggering pulse is applied at the base of Q1, the circuit goes into the quasi-stable state because $V_{B1} > V_{EN2}$. when Q1 goes ON its collector potential drops, Consequently a negative step is applied to the base of Q2 turning Q2 off. due to conduction of Q1, a voltage drop V_{EN1} is developed across R_E. In the quasi stable state, $V_{B1} > V_{EN1}$ and Q1 is ON and Q2 is OFF. however when Q1 is ON, the capacitor 'C' charges from V_{CC} through R. when the potential V_{BN2} reaches the value of $V_{EN1} + V_r$, the transistor Q2 conducts and due to regenerative feed back Q2 goes into saturation and Q1 into cut off and the pulse ends.

Astable Multivibrator :

As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two

quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are 2 types of astable multivibrators

1. Collector – coupled astable multivibrator.
2. Emitter-coupled astable multivibrator.

The Collector – coupled Astable multivibrator :

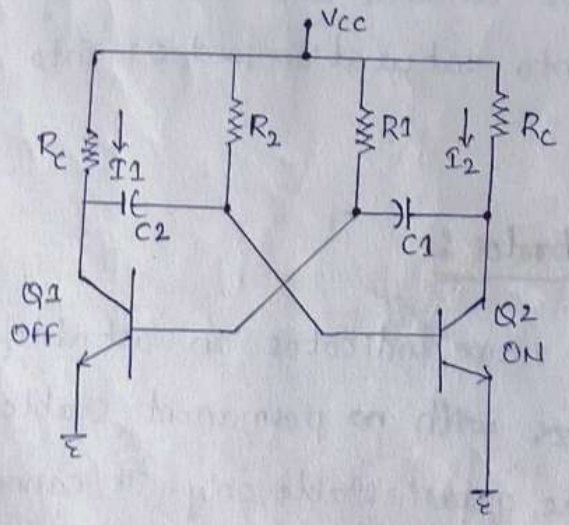


Figure shows the circuit diagram of a collector – coupled astable multivibrator using n-p-n transistors.

The collectors of both the transistors Q1 and Q2 are connected to the bases of the other transistors through the coupling capacitors C1 and C2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. NO triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one transistor will go into saturation and the other into cut-off and also due to capacitive couplings it keeps on oscillating between its two quasi stable states.

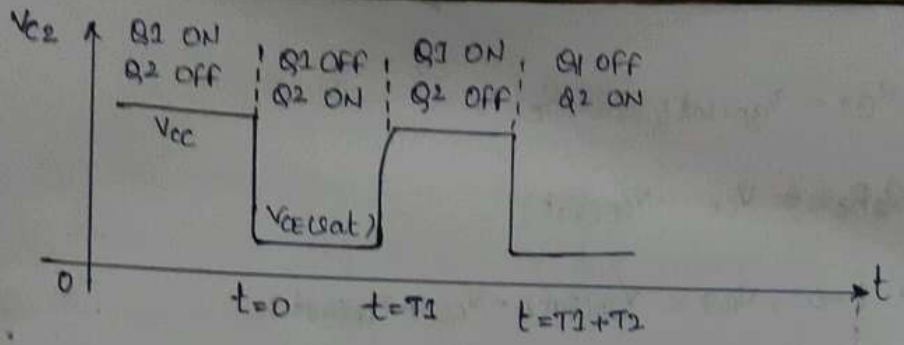
The waveforms at the bases and collectors for the astable multivibrator are shown below. At $t=0$, Q2 goes to ON state and Q1 to OFF state. So for $t<0$, Q2 was OFF and Q1 was ON. Hence for $t<0$, V_{B2} is negative, $V_{C2} = V_{CC}$, $V_{B1} = V_{BE(sat)}$ and $V_{C1} = V_{CE(sat)}$. The capacitor C2 charges from V_{CC} through R_2 and V_{B2} rises exponentially towards V_{CC}. At $t=0$, V_{B2} reaches the cut in voltage V_γ and Q2 conducts. As Q2 conducts, its collector voltage V_{C2} drops by $I_2R_C = V_{CC} - V_{CE(sat)}$

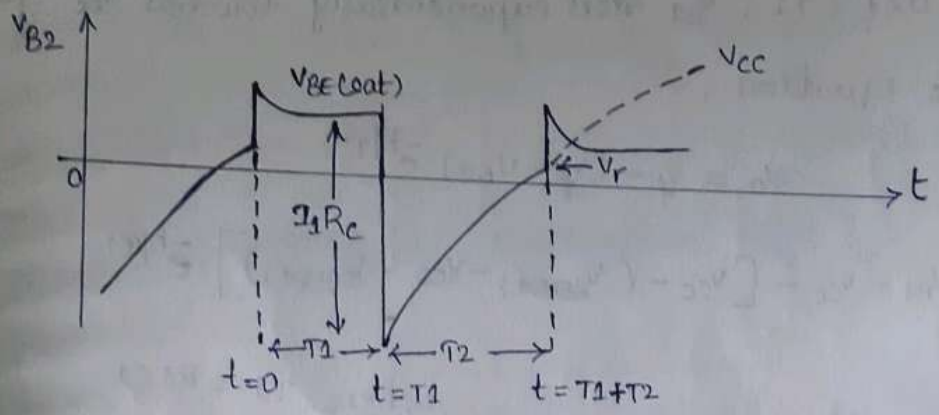
This drop in V_{C2} is transmitted to the base of Q1 through the coupling capacitor C1 to the base of Q1, causing an overshoot δ in V_{B1} and the abrupt rise by the same amount δ in V_{C1} as shown in figure. Now since Q2 is ON, C1 charges from Vcc through R1 and hence V_{B1} rises exponentially. At $t = T1$, when V_{B1} rises to V_γ, Q1 conducts and due to regenerative action Q1 goes into saturation and Q2 to cut-off. Now for $t > T1$, the coupling capacitor C2 charges from Vcc through R2 and at $t = T1 + T2$, when V_{B2} rises to the cut-in voltage V_γ, Q2 conducts and due to regenerative feedback Q2 goes to ON state and Q1 to off state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

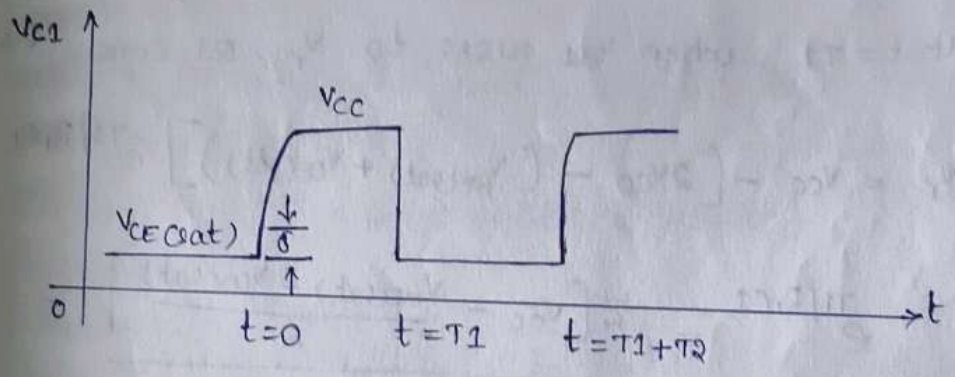
Expression for the frequency of oscillation of an astable multivibrator:

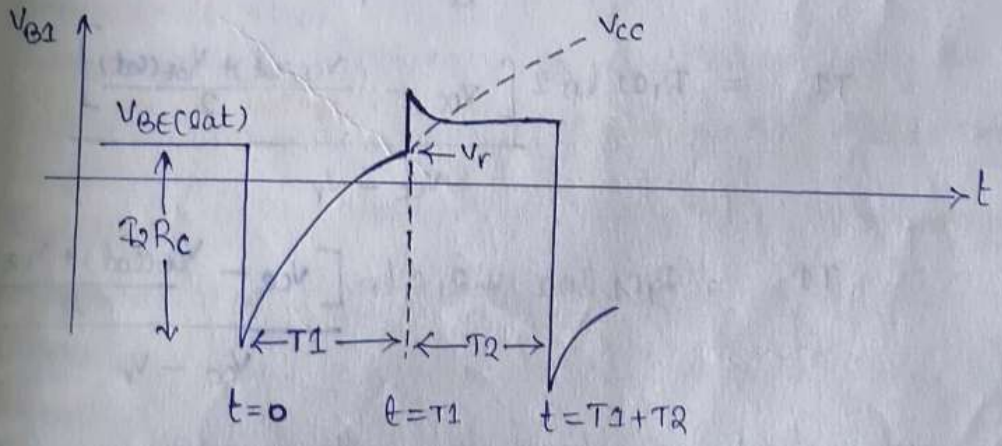
Consider the waveform at the base of Q1 shown in fig(d). At $t = 0$,

$$V_{B1} = V_{BE(sat)} - I_2 R_C$$


V_{C2}
Q1 ON
Q2 OFF
Q1 OFF
Q2 ON
Q1 ON
Q2 OFF
Q1 OFF
Q2 ON
V_{CC}
$V_{CE(sat)}$
0
t
t=0
t=T1
t=T1+T2


V_{B2}
$V_{BE(sat)}$
V_{CC}
V_r
I_1R_C
0
t
T1
T2
t=0
t=T1
t=T1+T2


V_{C1}
V_{CC}
$V_{CE(sat)}$
δ
0
t
t=0
t=T1
t=T1+T2


V_{B1}
V_{CC}
$V_{BE(sat)}$
V_r
I_2R_C
t
T1
T2
t=0
t=T1
t=T1+T2

$$V_{B1} = V_{BE(sat)} - I_2 R_c$$

but, $I_2 R_c = V_{cc} - V_{CE(sat)}$

At $t=0$, $V_{B1} = V_{BE(sat)} - V_{cc} + V_{CE(sat)}$

for $0 < t < T1$, V_{B1} rises exponentially towards V_{cc} given by the equation,

$$V_0 = V_f - (V_f - V_{0+}) e^{-t/\tau}$$

$$V_{B1} = V_{cc} - \left[V_{cc} - (V_{BE(sat)} - V_{cc} + V_{CE(sat)})\right] e^{-t/\tau_1}$$

where $\tau_1 = R_1 C_1$

At $t = T1$, when V_{B1} rises to V_r, Q1 conducts

$$V_r = V_{cc} - \left[2V_{cc} - (V_{BE(sat)} + V_{CE(sat)})\right] e^{-T1/R_1 C_1}$$

$$e^{T1/R_1 C_1} = \frac{2\left[V_{cc} - \frac{V_{BE(sat)} + V_{CE(sat)}}{2}\right]}{V_{cc} - V_r}$$

$$T1 = R_1 C_1 \ln \frac{2\left[V_{cc} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2}\right]}{V_{cc} - V_r}$$

(or)

$$T1 = R_1 C_1 \ln 2 + R_1 C_1 \ln \frac{\left[V_{cc} - \frac{V_{CE(sat)} + V_{BE(sat)}}{2}\right]}{V_{cc} - V_r}$$

At room temperature for a transistor

$$V_r = \frac{V_{CE(sat)} + V_{BE(sat)}}{2}$$

$$T1 = R_1C_1 \ln 2 = 0.693 R_1C_1$$

On similar lines considering the waveform of fig(b), we can show that the time T2 for which Q2 is off and Q1 is ON is given by

$$T2 = R_2C_2 \ln 2 = 0.693 R_2C_2$$

Total time period $T = T1 + T2 = 0.693(R_1C_1 + R_2C_2)$

The frequency of oscillation, $f = \frac{1}{T}$

$$f = \frac{1}{0.693(R_1C_1 + R_2C_2)}$$

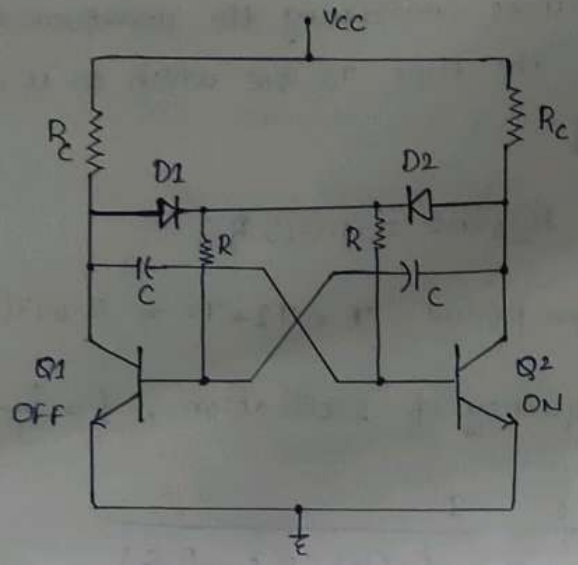
If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $T1 = T2 = T/2$

$$T = 2 \times 0.693RC = 1.386 RC$$

and $$f = \frac{1}{1.386 RC}$$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying RC. It is also possible to vary the frequency electrically by connecting R1 and R2 to an auxillary voltage source V (the collector supply remains $+V_{CC}$) and then varying this voltage V.

The astable multivibrator which does not block:

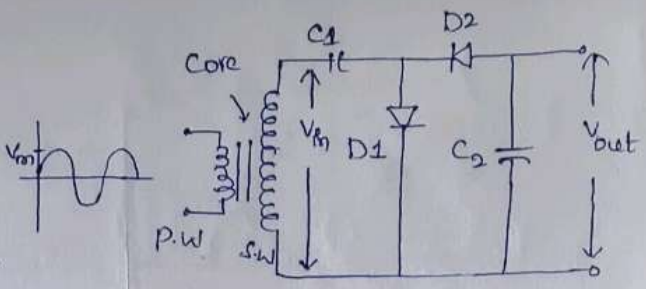


For the astable multivibrator shown in figure if the supply voltage is increased slowly from zero to its full value Vcc, both the transistors may go into saturation simultaneously and remain in that state. This "blocked condition" does not occur if the voltage is applied suddenly. A circuit which cannot block is shown in above circuit.

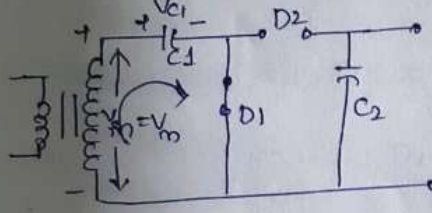
voltage multiplier circuits are used to maintain relatively low transfer peak voltage by stepping up the peak output voltage to 2, 3, 4 or more times the peak rectified voltage.

- voltage multiplier circuits
  - voltage doubler
    - Half wave voltage doubler
    - Full wave voltage doubler
  - voltage tripler & quadrapler

Halfwave voltage doubler

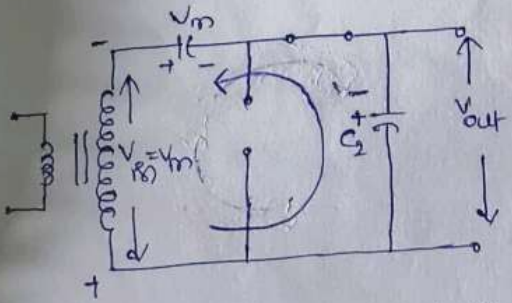


During the +ve half cycle D1 gets F.B and D2 gets R.B, as both the diodes are ideal

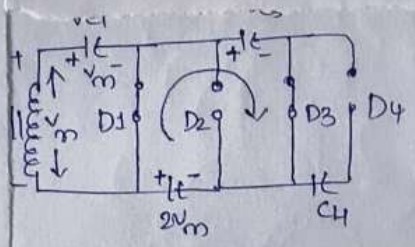


$V_m - V_{C1} = 0 \Rightarrow V_m - V_{C1} = 0 \Rightarrow V_{C1} = V_m$

During the -ve half cycle D1 gets R.B and D2 gets F.B, as both diodes are ideal

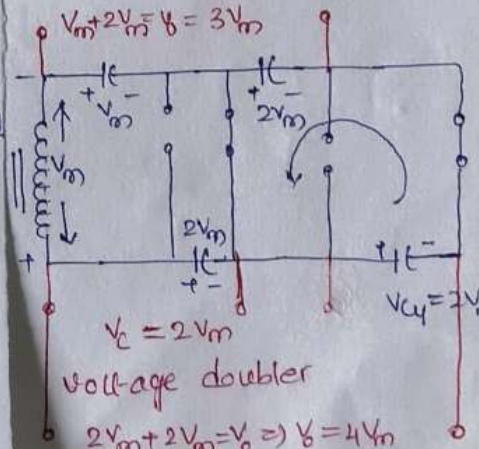


$V_{C2} - V_m - V_m = 0 \Rightarrow V_{C2} = V_m + V_m = 2V_m$



tripler

$V_m + 2V_m = V_0 = 3V_m$



$V_C = 2V_m$

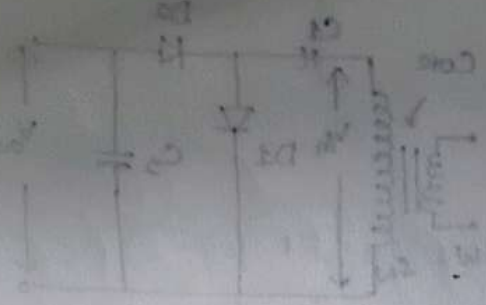
voltage doubler

$2V_m + 2V_m = V_0 \Rightarrow V_0 = 4V_m$

quadrapler

⇒ Von neumann architecture uses a single memory address for either program code or data, but not for both.

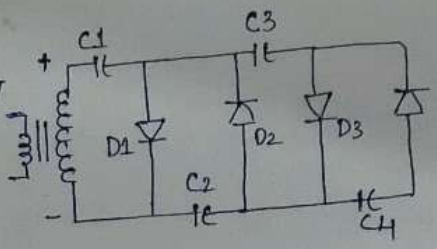
⇒ 8051 has harvard architecture which uses the same address, in different memories, for code and data.



value Vcc, both the
simultaneously and
condition" does not
A circuit which cann

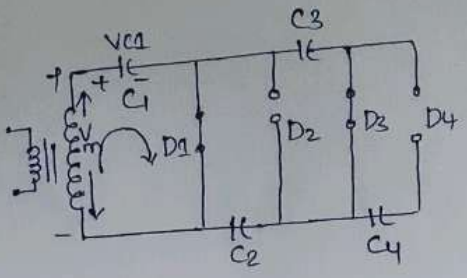
Voltage Tripler & quadrupler:

① for the 1st +ve half cycle



D1 → FB, D2 → RB, D3 → FB, D4 → RB

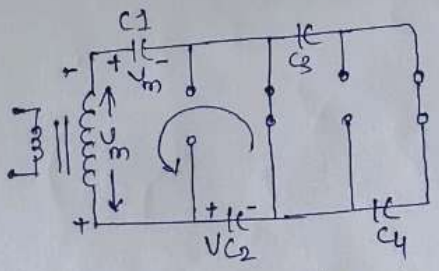
All are ideal diodes, so we have to replace them by their equivalent



$V_m - V_{C1} = 0$

$V_{C1} = V_m$

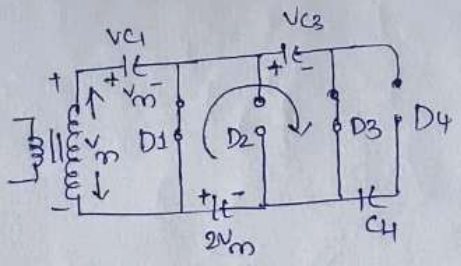
② for the 1st -ve half cycle



D1 → RB, D2 → FB, D3 → RB, D4 → FB

$-V_m - V_m + V_{C2} = 0 \Rightarrow V_{C2} = 2V_m$

③ for the 2nd +ve half cycle



D1 → FB, D2 → RB, D3 → FB, D4 → RB

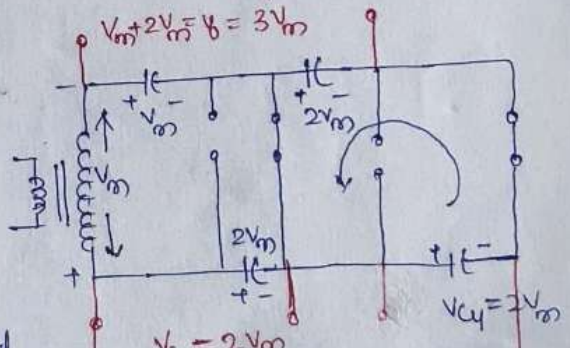
$-2V_m + V_{C3} = 0 \Rightarrow V_{C3} = 2V_m$

④ for the 2nd -ve half cycle

D1 → RB, D2 → FB, D3 → RB, D4 → FB

$-2V_m + V_{C4} = 0 \Rightarrow V_{C4} = 2V_m$

tripler



$V_c = 2V_m$

voltage doubler

$2V_m + 2V_m = V_0 \Rightarrow V_0 = 4V_m$

quadrapler

When 1st & 2nd capacitors are charged the ckt works as voltage doubler. when 1st, 2nd, 3rd capacitors are charged it will work as tripler and when all the capacitors are charged the ckt works as quadrapler.